A Rail-To-Rail Class-AB Amplifier With an Offset Cancellation for LCD Drivers

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Abstract—A rail-to-rail amplifier with an offset cancellation, which is suitable for high color depth and high-resolution liquid crystal display (LCD) drivers, is proposed. The amplifier incorporates dual complementary differential pairs, which are classified as main and auxiliary transconductance amplifiers, to obtain a full input voltage swing and an offset canceling capability. Both offset voltage and injection-induced error, due to the device mismatch and charge injection, respectively, are greatly reduced. The offset cancellation and charge conservation, which is used to reduce the dynamic power consumption, are operated during the same time slot so that the driving period does not need to increase. An experimental prototype amplifier is implemented with 0.35-μm CMOS technology. The circuit draws 7.5 μA to obtain a voltage swing of 5 V under a 3.4 kΩ resistance, and a 140 pF capacitance load with a power supply of 5 V. The offset voltage of the amplifier with offset cancellation is 0.48 mV.

Index Terms—Amplifier, class-AB amplifier, liquid-crystal display, liquid-crystal display driver, offset cancellation, rail-to-rail amplifier.

I. INTRODUCTION

WITH the revolutionary advancement of LCDs, there is a large demand for developing high-resolution and high color depth driver ICs [1]–[8]. LCD panels on multimedia products have become larger with higher definition, and their color quality requires more accuracy. For LCD-TV applications, the drivers must convert 10-bit digital input codes to analog levels, at which point the built-in buffer amplifiers drive the data lines [9]–[11]. The buffer amplifiers determine the speed, resolution, voltage swing, and power dissipation of the LCD drivers [3]–[7]. In a high-quality display module, the amplifier has a higher resolution, and it should offer an almost rail-to-rail voltage driving to accommodate higher gray levels. The settling time should be smaller than the horizontal scanning time. Also, the offset voltage should be greatly reduced to achieve high color depth.

Amplifiers for LCD applications have been proposed and demonstrated in recent work. For example, Ito et al. [12] proposed a rail-to-rail class-AB amplifier for LCD drivers, in which the number of current paths is reduced and the phase compensation is suitable for high-speed operation. Weng et al. [13] proposed a compact, low-power, and rail-to-rail class-B output buffer for driving the large column line capacitance of LCDs, in which a nonlinear element in the feedback path is modified from the current-mirror amplifier to obtain area and power advantages. Lu [14] proposed a high-speed driving scheme and a compact high-speed low-power rail-to-rail class-B buffer amplifier, which are suitable for both small- and large-size LCD applications. Hong [18] proposed a low offset high voltage swing rail-to-rail buffer amplifier for LCD driver, in which the nonlinearity of the output voltage is reduced.

Mismatch of the devices causes an offset voltage, which limits the high-resolution for LCD driver application. Some methods are proposed to reduce the offset voltage. For example, “output offset storage” and “input offset storage” techniques measure the offset voltage and store the result on capacitors in series with the output/input. However, these two techniques introduce capacitors in the signal path, a particularly serious issue in op-amps and feedback system. To resolve the above issues, an offset cancellation scheme, which can isolate the signal path from the offset storage capacitors through the use of an auxiliary amplifier, was proposed [16]. A push-pull stage is often used as an output stage in CMOS buffer amplifiers. The push-pull stage consists of two complementary common-source transistors, allowing rail-to-rail output voltage swing. The gates of the two output transistors are normally driven by two in-phase ac signals separated by a dc voltage [16]. To drive the output transistors, a slew rate enhancement circuit or a level shifter is added in some amplifiers [5], [17]. However, this scheme uses more current paths. Hence, to achieve a rail-to-tail input/output voltage swing operation with offset cancellation, an extra rail-to-rail differential amplifier and a slew rate enhancement/level shifter are needed in the conventional amplifier, thus increasing the die area and the power consumption.

In this work, dual single-ended amplifiers are used to drive the two output devices, achieving the offset cancellation and the push-pull driving. Since no extra current paths are needed for the class-AB operation, this amplifier consumes less current and occupies smaller die area. The single-ended amplifier incorporates a complementary differential pair as the input stage, to obtain a full input voltage swing and an offset canceling function. The offset voltage, which is due to the process and mismatch variation, is greatly reduced. The injection-induced error of the switched-capacitor amplifier can be reduced by selecting the proper size ratio of the differential amplifiers. The offset cancellation and charge conservation, used to reduce the dynamic power consumption, are operated during the same time slot so that the driving period does not need to increase.
II. PROPOSED AMPLIFIER

To reduce costs, some low-resolution driver ICs do not employ the offset cancellation technique. However, this technique is recommended in high-quality driver ICs. Amplifiers without and with offset cancellation are described in this section, in subsection A and B, respectively.

A. Proposed Amplifier Without Offset Cancellation

The architecture of the proposed two-stage buffer amplifier, shown in Fig. 1, consists of 1) four transconductance amplifiers, Gmap, Gmn, Gmp, and Gman; 2) two transimpedance amplifiers, R1 and R2; and 3) a pair of complementary common-source amplifiers, M25 and M26. The four transconductance amplifiers are dual complementary differential pairs, which, along with the two transimpedance amplifiers, compose the first stage. Gmn and Gmp are main transconductance amplifiers, and Gmap and Gman are auxiliary transconductance amplifiers. Gmn and Gmap, which are NMOS input and PMOS input differential pairs, are actively loaded by R1, while Gmp and Gman are actively loaded by R2. The complementary common-source amplifiers, M25 and M26, are used to drive the data line of the LCD panel as the second stage. To achieve the push-pull driving, dual single-ended amplifiers are used to drive the output devices. The single-ended amplifier incorporates a complementary differential pair as the input stage, to obtain a full input voltage swing. The main and auxiliary transconductance amplifiers are dual complementary differential pairs; thus, when the input voltage is near to rail voltages, one of the main transconductance amplifiers is cut off although its counterpart auxiliary transconductance amplifier still operates. For example, as the input voltage is near to the value of VDD, Gmp and Gmap are cut off, but Gmn and Gman can amplify the input signal to the output stage through R1 and R2, respectively. Hence, the architecture is a rail-to-rail amplifier.

The equivalent circuit of the proposed two-stage amplifier is shown in Fig. 2, where $g_{m1}$ and $g_{m2}$, $R_{c1}$ and $R_{c2}$, and $C_{o1}$ and $C_{o2}$ are the transconductances, output resistances, and output parasitic capacitances of the first-stage and second-stage amplifiers, respectively. $C_{cs}$ and $R_{cs}$ are used for the stability. The data line of the LCD panel is an $R - C$ distribution. To simplify the small-signal analysis, the data line is modeled as a first-order $R - C$ circuit. Since the first-stage amplifier contains dual complementary differential pairs, the value of $g_{m1}$ depends on the input common-mode voltage. To evaluate this value of $g_{m1}$, the input voltage is divided into low, middle, and high levels. When the input voltage is at the low level, the PMOS input transconductance amplifiers are operating and the NMOS input transconductance amplifiers are cut off, and vice versa for the high-level inputs. All transconductance amplifiers can amplify the input signal when the input voltage is at the middle level. Hence, the value of $g_{m1}$ can be expressed as

$$g_{m1} = g_{mn} + g_{man}$$

as the input voltage is at the high level;

$$g_{map} + g_{mn} + g_{mp} + g_{man}$$

as the input voltage is at the middle level;

$$g_{map} + g_{mp}$$

as the input voltage is at the low level

$$\text{(1)}$$

where $g_{mn}, g_{man}, g_{map}, g_{mp}$ are the transconductances of the transconductance amplifiers, $G_{mn}, G_{map}, G_{mp}, G_{man}$, respectively. Since the transconductance of the first stage amplifier varies with the input common-mode voltage, the dc gain of the amplifier varies over the signal swing for large signals. The distortion will then be generated in a continuously large signal. To reduce the distortion encountered due to this variation, the input stage should be modified to a rail-to-rail constant $gm$ differential amplifier. For an LCD driver application, the amplifier is used to buffer the step-wise signals. Hence, the constant $gm$ design is not required.

The open-loop transfer function, $A_o(s)$, can be obtained from Fig. 2 and the assumptions: $C_{o1}, C_{o2} < C_{cs} < C_L; R_{o1}, R_{o2} > R_{cs}, R_L$; and $g_{m2}R_L < 1$. That is:

$$A_o(s) = \frac{v_{out}(s)}{v_{id}(s)} = \frac{A_{ck}}{1 + \frac{s}{\omega_{z1}}} \left( \frac{1 + \frac{s}{\omega_{z2}}}{1 + \frac{s}{\omega_{z3}}} \right) \left( \frac{1 + \frac{s}{\omega_{z4}}}{1 + \frac{s}{\omega_{z5}}} \right)$$

$$\text{(2)}$$

where

$$A_{ck} = \frac{g_{m1}g_{m2}R_{o1}R_{o2}}{C_L}$$

$$\omega_{z1} = \frac{1}{C_L R_L}$$

$$\omega_{z2} = \frac{1}{C_{cs}(R_{cs} - 1/g_{m2})}$$

$$\omega_{z3} \approx \frac{1}{C_{cs}(g_{m2}R_{o2})R_{o1} + C_L R_{o2}}$$

$$\text{(3)}$$

$$\text{(4)}$$

$$\text{(5)}$$

$$\text{(6)}$$
The zeros at $\omega_{z1}$ and $\omega_{z2}$ are contributed by the distributed $R-C$ load and the Miller compensation, respectively. The dominant pole, $\omega_{p1}$, is due to the Miller compensation and the distributed $R-C$ load. The first term of the denominator in (6) is arisen at the interface between the first and second stages. The output resistance of the first stage, $R_{o1}$, is interacting with the Miller capacitance, $C_{cs}(g_{m2}R_{o2})$ at the interface. The second term is due to the output resistance of the second stage and the load capacitance. Since the load capacitance of the LCD data line can be the order of hundred pico-farads, the second term, $C_{L}R_{o2}$, can not be neglected in the LCD driver application. The second nondominant pole, $\omega_{p2}$, is arisen at the output of the second stage amplifier with the Miller effect. For a conventional two-stage operational amplifier, the first term of the numerator in (7) is much smaller than the second one, resulting to that $\omega_{p2} \approx g_{m2}/C_{L}$. That is: $\omega_{p2}$ is determined by the transconductance of the second stage amplifier and the load capacitance. Here, for the LCD driver application, the load capacitance can not be neglected. If $C_{L}$ is much greater than $C_{cs}(g_{m2}R_{o1})$, $\omega_{p2}$ can be approximated expressed as: $1/C_{cs}R_{o1}$, which is independent on the transconductance of the second stage amplifier and the load capacitance. The third and fourth nondominant poles, $\omega_{p3}$ and $\omega_{p4}$, due to the parasitic capacitances, are far away from the other poles and zeros. Hence, they have less effect on the stability. The unity-gain frequency can be approximately expressed as

$$\omega_{u} \approx A_{bi} \omega_{p1} \approx \frac{g_{m0}g_{m2}R_{o2}}{C_{cs}(g_{m2}R_{o2})R_{o1} + C_{L}R_{o2}}$$ (10)

which is larger than the pole at $\omega_{p2}$. Hence, the actual value of the unity-gain frequency is slightly smaller than that of (10). The position of $\omega_{z1}$ is greatly affected by the $R-C$ load. The larger the load connected to the amplifier, the smaller the value of $\omega_{z1}$, decreasing to less than the unity-gain frequency for a large load. The values of $\omega_{p1}$ and $\omega_{u}$ are also greatly affected by the load capacitance. As depicted in Fig. 3(a), which shows an open-loop frequency characteristic of the amplifier with a large load, the phase shift of $\omega_{p2}$ is compensated for by $\omega_{z1}$. As $C_{L}$ is increased, $\omega_{p1}$ and $\omega_{u}$ are reduced, resulting in the increment of the phase margin. This means that a sufficient phase margin can be obtained even for a small value of the compensation capacitor. Also, the compensation resistor, $R_{cs}$, is not needed to drive the medium- or large-size LCD panels. For this case ($R_{cs} = 0$), $\omega_{z2}$ is located at the positive S-half plane. However, since the value of $C_{cs}$ is small, the value of $\omega_{z2}$ is much larger than the unity-gain frequency, resulting in a smaller decrease of the phase margin. However, for a small-size LCD panel, the values of $R_{L}$ and $C_{L}$ are lower, and $\omega_{p2}$ and $\omega_{z3}$ move toward to the right on the open-loop frequency characteristic curve. The position of $\omega_{z1}$ may be moved to the right of the unity-gain frequency, but $\omega_{p2}$ remains to the left. This results in a reduction of the phase margin. Fig. 3(b) depicts the open-loop frequency characteristic of the amplifier with a small load. To compensate for the frequency response for this small distributed $R-C$ load, $R_{cs}$ is needed to move the zero at $\omega_{p2}$ to the negative S-half plane to increase the phase margin. Selecting an adequate value of $R_{cs}$ can result in sufficient phase margin for a small $R-C$ load. However, trying to cancel $\omega_{p2}$ with $\omega_{z3}$ in this manner can lead to doublts resulting in slow settling tails. Fortunately, the settling time requirement of the small-size LCD panel is not strict as that of the large-size LCD. An alternative compensation scheme can be used for a small load application: inserting a resistor between the output of the amplifier and the load [1]. However, this will reduce the slew rate.

The schematic of the proposed amplifier without offset cancellation is shown in Fig. 4. The transistors M1-M3, M4-M6, M7-M9 and M10-M12 compose the transconductance amplifiers Gmap, Gmn, Gmp, and Gman, respectively. Their transimpedance amplifiers R1 and R2 are composed of M13-M18 and M19-M24, respectively. Mr1-Mr4, which are connected as two transmission gates, are used as the compensation resistors. As described above, the compensation resistors can be removed for driving a large-$RC$ distributed load. So that the proposed amplifier can drive both small- and large-$RC$ distributed loads, the compensation resistors are included in the circuit. $C_{cs1}$ and $C_{cs2}$ are the compensation capacitors. The letters A-H are used to indicate the line connection, and $V_{11}$, $V_{12}$, $V_{13}$ and $V_{14}$ are the bias voltages. The current mirror, M13 and M14, is the active load of the differential pair of M4 and M5. To sum the signal currents of the two differential pairs, M2–M5, a folded circuit, M15–M18, is added in the resistance amplifier, R1. M17 and M18 are used for supplying the dc currents for this resistance amplifier. M15 and M16, which are the common-gate amplifiers, are used to
transfer the differential signals of M2 and M3 to M13 and M14. A symmetric schematic is designed in the resistance amplifier, R2.

To avoid the transistors, M17–M20, entering into the triode region, the gate voltages of M15, M16, M21, and M22 should be carefully designed. In this work, the gates of M15 and M16 are biased at the voltage of $V_{GS15} - V_{GS17}$. Similarly, a voltage of $V_{DD} - V_{SG19} - V_{SG21}$ is applied to the gates of M21 and M22. These bias voltages can be easily implemented. Mb1–Mb8 and Rb, constitutes the bias circuit [19], which provides the bias currents independent of both the supply voltage and the MOSFET threshold voltage. The sizes of Mb7 and Mb8 are deliberately designed to be mismatched, with Mb8 usually about four times wider than Mb7. A resistor Rb is connected in series with the source of Mb8. The value of Rb determines the bias current, $I_B$. To bias the gates of M15 and M16, a cascode transistor Mb6 and a matched diode-connected transistor Mb5 are included. Finally, a p-channel cascode current mirror formed by two pairs of matched devices, Mb1–Mb4, replicates the current $I_B$ back to Mb5 and Mb7, as well as providing the bias voltages for M1, M7 and M19–M22.

In the stable state, the dc current of the output stage is biased by the two resistance amplifiers, R1 and R2. The currents flowing in M14 and M24 can be expressed as

$$I_{14} = I_{38} - I_2 + I_4$$
$$I_{24} = I_{29} - I_{10} + I_8$$

where $I_i$ and $(W/L)_i$ indicate the dc current and the aspect ratio of the device $i$, respectively. If the input stage is perfectly balanced, the voltage appearing at the drain of M14 equals to that at its gate. Thus the dc current of M25, $I_{25}$, is related to the current of M14 by the relationship

$$I_{25} = \frac{(W/L)_{25}}{(W/L)_{14}} I_{14}$$
$$= \frac{(W/L)_{25}}{(W/L)_{14}} \left[ \frac{(W/L)_{38}}{(W/L)_{61}} - \frac{1}{2} \frac{(W/L)_{12}}{(W/L)_{67}} + \frac{1}{2} \frac{(W/L)_{7}}{(W/L)_{61}} \right] I_B$$

Similarly, the dc current of M26, $I_{26}$, is related to M24 by

$$I_{26} = \frac{(W/L)_{26}}{(W/L)_{24}} I_{24}$$
$$= \frac{(W/L)_{26}}{(W/L)_{24}} \left[ \frac{(W/L)_{20}}{(W/L)_{61}} - \frac{1}{2} \frac{(W/L)_{12}}{(W/L)_{67}} + \frac{1}{2} \frac{(W/L)_{7}}{(W/L)_{61}} \right] I_B$$

In order for no systematic offset voltage to appear at the output, this sink current, $I_{26}$, must be equal to the current supplied by M25.

As a buffer, the output is connected to the inverting input terminal (in–), and the input signal is applied to the non-inverting input terminal (in+). The data line of the LCD panel is connected to the output labeled “out”. When the non-inverting input voltage, in+, is reduced, the gate voltages of M25 and M26 are increased. As a result, M26 starts to discharge the output node. When the output voltage reaches the level that the voltage difference between the input and output is almost zero, M26 stops discharging the output node. Similarly, when the input voltage, in+, is increased, M25 charges the output load until the output voltage almost equals to the input voltage.

The class-AB behavior, which is simulated in a 0.35 μm CMOS technology with the device parameters shown in Table I by the circuit simulator Hspice, is shown in Fig. 5 where the maximum signal current of M25 that can be delivered to the load is 1.2 mA but the quiescent current is only 1.8 μA. The ratio between the maximum signal current and the quiescent current is 666.

The device mismatch may introduce the offset voltage and dissipate more output current. The proposed offset cancellation scheme, which will be described in the sub-section B, is used to reduce the offset voltage. The output transistors will dissipate more static current at the cross corner of fast-PMOS and fast-NMOS. Also, the quiescent current of the output transistors may have a large variation due to the random input-referred offset voltage of the first stage. That is, an opposite bias level shift at the gate-to-source voltages of the output transistors will induce more quiescent current. This problem can be solved by intentionally introducing an offset voltage into the two single-ended amplifiers in such a way that the output transistors are not carrying any current in the quiescent state. The proposed circuit then becomes a class-B amplifier. The class-B amplifier

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Fig. 3. Open-loop frequency characteristic of the amplifier with (a) a large load and (b) a small load, respectively.
has a crossover distortion problem, which is a major disadvantage for processing continuous signal. Since the proposed amplifier is used to buffer the step-wise signal in the LCD driver, the distortion is less important [4].

The transconductance and transimpedance amplifiers form the first stage, in which the transimpedance amplifiers combine the currents of the main and auxiliary transconductance amplifiers to achieve the rail-to-rail input operation. Since the transconductance of the first stage varies with the input common-mode voltage, the phase margin will be different for low, high and middle level signals. Fig. 6(a), (b) and (c) show the simulated phase margins of the proposed amplifier with compensation resistors for low (0 V), high (5 V) and middle (2.5 V) input levels, respectively. The simulated phase margins of the amplifier without compensation resistors for low, high and middle input levels are shown in Fig. 7(a), (b) and (c), respectively. They can be seen that the amplifier has a large enough phase margin for driving a large load even without the compensation resistors. However, the compensation resistors are needed to improve the stability for a small load. The equivalent values of the resistance and capacitance of the data line

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<th>Device Sizes Used in the Amplifier</th>
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Fig. 6. Simulated phase margins of the proposed amplifier with compensation resistors for (a) low (0 V), (b) high (5 V) and (c) middle (2.5 V) input levels, respectively.

Fig. 7. Simulated phase margins of the amplifier without compensation resistors for (a) low (0 V), (b) high (5 V) and (c) middle (2.5 V) input levels, respectively.

for a sub-pixel are 2.406 Ω and 113.35 fF, respectively [15]. For a Quarter VGA (RGB × 320 × 240), the total values of the resistance and capacitance of the data line are 577 Ω and 27.2 pF, respectively. From Fig. 6(c), it can be seen that the phase margin increases from 31° to 47° for a middle input level when the compensation resistors are inserted between the two stages of the amplifier. The phase margin can be further increased by increasing the bias current of the amplifier or by inserting a resistor between the output of the amplifier and
the data line. For a QUXGA (RGB × 3200 × 2400), the total values of the resistance and capacitance of the data line are 5.77 kΩ and 272 pF, respectively. The phase margins of the amplifier with and without compensation resistors are 109° and 80°, respectively. Hence, the compensation resistors can be removed from an amplifier driving a large load.

As described above, the compensation resistors are needed for a small load. The smaller load, the larger value of the compensation resistor is required. Due to several hundreds of buffer amplifiers are built into a single LCD source driver IC, the amplifier should occupy a small die area. To reduce the die area, the transmission gates are used as the compensation resistors in this amplifier. Since the gates of the transmission gates are connected to both VDD and ground, the noise may be injected to the output of the amplifier from the noisy power lines. The simulated power supply reject ratios (PSRR), in which the amplifier with transmission gates and ideal resistors is simulated, respectively, are shown in Fig. 8. They can be seen that the amplifier has almost the same values of PSRR for transmission gates and ideal resistors below 1 MHz. The power supply noise is mainly injected through the current mirrors (M13–M14 and M23–M24) at low frequencies [20]. Hence, the transmission gates can be used as the compensation resistors without significantly reducing the PSRR.

B. Proposed Amplifier With Offset Cancellation

As described in the previous sub-section, the auxiliary transconductance amplifiers are used to extend the input swing. They can also be used for the offset cancellation. The architecture of the proposed amplifier with an offset cancellation is shown in Fig. 9, where an offset storage capacitor and three switches are used in the circuit, and \( V_{\text{OS1}} \), \( V_{\text{OS2}} \), \( V_{\text{OS3}} \), and \( V_{\text{OS4}} \) are the input-referred offset voltages of \( G_{\text{mn}} \), \( G_{\text{mp}} \), \( G_{\text{map}} \), and \( G_{\text{man}} \), respectively. Since the input stage contains both PMOS and NMOS differential amplifiers, the offset voltage varies with the input voltage. For the LCD driver application, a step-wise signal is applied to the input of the buffer amplifier. Hence, the buffer amplifier must sample each voltage level for the offset cancellation. The operation is divided into offset cancellation and driving phases. Before each driving phase, the amplifier is in the offset cancellation phase, the switches SW2 and SW3 are turned on, and the switch SW1 is turned off. After the offset cancellation is finished, SW1 is turned on and SW2 and SW3 are turned off. The circuit is then ready to drive its load.

During the offset cancellation phase, a negative feedback loop consisting of the auxiliary transconductance amplifiers, \( G_{\text{map}} \) and \( G_{\text{man}} \), the transimpedance amplifiers, \( R_1 \) and \( R_2 \), and the output transistors, M25 and M26, is formed. The input voltage is applied to the inverting input terminals of all transconductance amplifiers and to the non-inverting input terminals of the two main transconductance amplifiers. As depicted in Fig. 9, the input-referred offset voltages, \( V_{\text{OS1}} \) and \( V_{\text{OS2}} \), are applied to the two inputs of \( G_{\text{mn}} \) and \( G_{\text{mp}} \), respectively. The relation between the input and output voltages can be expressed as

\[
\begin{align*}
{[\pm V_{\text{OS1}} g_{m\text{in}} & + (V_{\text{out}} - V_{\text{in}} \pm V_{\text{OS3}}) g_{m\text{mp}}]} R_1 g_{m25} \\
+ [\pm V_{\text{OS2}} g_{m\text{mp}} & + (V_{\text{out}} - V_{\text{in}} \pm V_{\text{OS4}}) g_{m\text{man}}]} R_2 g_{m26}\end{align*}
\]

\[
R_{\text{out}} = V_{\text{out}}
\]

(15)

where \( g_{m25} \) and \( g_{m26} \) are the transconductances of M25 and M26, respectively, and \( R_{\text{out}} \) is the output resistance of the amplifier.

Fig. 8. Simulated power supply reject ratios.

Fig. 9. Architecture of the proposed buffer amplifier with an offset cancellation.
Thus (see (16) at the bottom of the page). Assuming that $g_{m25} = g_{m26}$ and $R_1 = R_2$, the output voltage can be expressed as

$$V_{out} \approx V_{in} + \frac{\pm V_{OS1}f_{mn} \pm V_{OS2}f_{mp} \pm V_{OS3}f_{mp} \pm V_{OS4}f_{man}}{g_{map} + g_{man}}.$$  \hspace{1cm} (17)

The output voltage is stored on the storage capacitor $C_s$ after the switches SW2 and SW3 are turned off and the switch SW1 is turned on. Then, the output offset voltage is

$$V_{out} - V_{in} \approx \frac{\pm V_{OS1}f_{mn} \pm V_{OS2}f_{mp} \pm V_{OS3}f_{mp} \pm V_{OS4}f_{man}}{g_{map} + g_{man}}.$$  \hspace{1cm} (18)

The offset voltage referred to the input is therefore given by

$$V_{OS, tot} = \frac{V_{out} - V_{in}}{A_{dc}}$$
$$= \frac{\pm V_{OS1}f_{mn} \pm V_{OS2}f_{mp} \pm V_{OS3}f_{mp} \pm V_{OS4}f_{man}}{(g_{map} + g_{man})A_{dc}}.$$  \hspace{1cm} (19)

where $A_{dc}$ is the DC gain of the amplifier. Its value is usually on the order of 80 dB. Hence, the offset voltage due to the device mismatch is greatly reduced to a very small value.

As the conventional offset cancellation, the switch SW2 will introduce an injection-induced error. The resulting input-referred offset voltage can be expressed as

$$V_{OS, inj} = \left(\frac{g_{map} + g_{man}}{g_{mn} + g_{mp}}\right)\Delta V$$  \hspace{1cm} (20)

where $\Delta V$ is the injection-induced error voltage on the storage capacitor. To reduce this error, the transconductances of the main transconductance amplifiers can be designed to be larger than those of the auxiliary amplifiers. The schematic of the proposed amplifier with offset cancellation is shown in Fig. 10, where the switches are implemented by the transmission gates.

Charge conservation technology, which is shown in Fig. 11, is usually used to reduce the power consumption by reducing the average voltage swing. The voltage level refresh of the data lines is divided to three phases. In the first phase, all data lines are isolated from the outputs of the buffers. In the second phase, they are shorted to an external capacitor, $C_{ext}$. These first two phases are used for the charge conservation of the data lines. In the last phase, all data lines are connected to their corresponding buffer amplifiers, and the buffer amplifiers continue to drive the data lines to their final values. The charge conservation phase
can also be used for the offset cancellation of the proposed amplifier, eliminating the need for an additional phase for offset cancellation. Thus, the driving time does not need to increase.

### III. EXPERIMENTAL RESULTS

The proposed amplifiers without and with offset cancellation were fabricated using a 0.35-μm CMOS technology. Their die photographs are shown in Fig. 12(a) and (b), respectively, and their areas are $125 \times 48 \mu m^2$ and $175 \times 48 \mu m^2$. The active area of the amplifier is $103 \times 40 \mu m^2$. If the amplifier is used to drive medium- or large-size LCD panels, the compensation resistors are not needed and the die areas can be reduced.

The measured results of the amplifier, which is connected as a buffer, without offset cancellation are demonstrated first. A quiescent current consumption of $7.5 \mu A$ is measured at a power supply of 5 V. Fig. 13 shows the measured results of the proposed amplifier output, with an input of a large dynamic range (0–5 V) 50 KHz triangular wave. The amplifier is loaded with the parasitic capacitances of the pad, die package and measurement equipment, with a total value of about 18 pF. The upper trace is the input waveform and the lower one is the output waveform. It can be seen that the output basically follows the input for a full swing. Hence, the proposed circuit is a rail-to-rail amplifier. The step response of the proposed amplifier, loaded with the parasitic capacitances of the pad, die package and measurement equipment with voltage swings of 20 mV and 5 V, are shown in Figs. 14 and 15, respectively. It can be seen that the buffer can be stable even if the load capacitance is as small as 18 pF. In order to show the performance of the amplifier, Fig. 16 shows the same measurement for a much larger load capacitance of 470 pF. The slew rates are 2.94 V/μs and 4.02 V/μs for the rising and falling edges, respectively. Fig. 17 shows the measured slew rates for different load capacitances.

The data line of the LCD panel is an $R-C$ distribution. A 5th-order $R-C$ configuration, which is shown in Fig. 18, is also used for the measurement. The total resistance and capacitance...
are $R_L$ and $C_L$, respectively, i.e., $R_L = 5R$ and $C_L = 5C$. The larger the panel size, the larger the values of $R_L$ and $C_L$. The 5-V step response of the buffer amplifier, loaded with $R_L = 3.4$ kΩ and $C_L = 140$ pF, is shown in Fig. 19, where the settling time to settle within 0.2% of the final voltage is 3 μs. For a UXGA (RGB × 1600 × 1200) display, the values of the total resistance and capacitance of the data line are 2.89 kΩ and 136 pF [15], respectively, and its horizontal scanning time is 9.877 μs. Hence, this circuit can be used for a UXGA LCD.

The buffer amplifier with offset cancellation is now demonstrated. To quickly sense the offset voltage, the data line should be disconnected from the buffer. Fig. 20 shows the 5-V step response of the buffer without resistance and capacitance loads. The upper curve is the input signal, the middle signal is the output response, and the bottom signal is the clock. The frequency of the clock signal is 100 KHz and the duty cycle is 20%, i.e., the offset cancellation and driving periods are 2 μs and 8 μs, respectively. The period of the offset cancellation can...
also be used for charge conservation. The offset measurements of the amplifier without and with offset cancellation are shown in Fig. 21(a) and (b), respectively. Since measurements of small differences between smaller values are more accurate, a voltage of 0 V is applied to the inputs of the amplifiers for the offset measurements. The accuracies, which are calculated from the data sheet of the measurement equipment [21], are 3.84 and 0.192 mV for the scales of 20 mV/div and 1 mV/div, respectively. The offset voltage is reduced from 70 mV to 0.48 mV, which is much smaller than that of the previous circuit [18]. The measured offset voltage is mainly due to the charge injection. In this prototype amplifier, a device ratio of 2 between the main and auxiliary transconductance amplifiers is designed to reduce the injection-induced error. As described in Subsection B of Section 2, this error voltage can be further reduced by increasing this device ratio. The increments in the area and power consumption caused by adding the auxiliary amplifiers and the offset storage capacitors are 40% and 17%, respectively. The performance of the proposed amplifier is summarized and compared with other circuits in Table II.

In order to improve the lifetime of the liquid crystal material, the liquid crystal of active matrix liquid crystal displays (AMLCD) should be driven by the so-called inversion method, which alternates the positive and negative polarities between the liquid-crystal cells with respect to a common backside electrode. Four inversion methods are used for AMLCD driving: frame, line, column and dot inversions. For the line and dot inversions, the backside electrode is at a fixed voltage and a negative-to-positive or positive-to-negative voltage with respect to the fixed voltage of the backside electrode must be driven from the LCD source drivers [2], [6]. Hence, the LCD driver IC should supply both positive and negative polarity voltages for a digital sub-pixel code. The preceding function block of the buffer amplifier is the digital-to-analog converter (DAC). Since the driver IC should supply both positive and negative voltages, the resolution of the DAC is increased by one bit. For a 10-bit 5-V source driver with the line/dot inversion, one LSB voltage is about 2.4 mV. Since the offset voltage of the amplifier with offset cancellation is smaller than 1/2 LSB voltage, the proposed amplifier is suitable for a 10-bit source driver application.

IV. CONCLUSION

This work presents a rail-to-rail class-AB amplifier with an offset canceling technology, which is suitable for high color depth and high-resolution LCD drivers. Dual complementary differential pairs are employed to obtain a rail-to-rail input and to cancel the offset voltage. Both offset voltage and injection-induced error, which are due to device mismatch and charge injection, respectively, are greatly reduced. The offset cancellation and charge conservation, used to reduce the dynamic power consumption, are operated during the same time slot so that the driving period does not need to increase. An experimental prototype rail-to-rail class-AB amplifier is implemented with 0.35-μm CMOS technology. The circuit draws 7.5 μA static current and exhibits the settling time of 3 μs for settling within 0.2% of the final voltage, for a voltage swing of 5 V under a 3.4 kΩ and a 140 pF capacitance load with a power supply of 5 V. The offset voltage of the amplifier with offset cancellation is 0.48 mV, which is mainly due to the charge injection. The offset
voltage can be further reduced by increasing the device ratio between the main and auxiliary transconductance amplifiers. The active area of this amplifier is 103.40 m². The measured data show that the proposed amplifier is very suitable for high color depth and high-resolution LCD drivers.

**ACKNOWLEDGMENT**

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**REFERENCES**


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### Table II

**Performance Summary**

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>Ito’s amplifier [12]</th>
<th>Weng’s amplifier [13]</th>
<th>Hong’s amplifier [18]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process technology</strong></td>
<td>0.35 μm CMOS</td>
<td>0.13 μm CMOS</td>
<td>0.35 μm CMOS</td>
<td>0.35 μm CMOS</td>
</tr>
<tr>
<td><strong>VDD</strong></td>
<td>5 V</td>
<td>5 V</td>
<td>3.3 V</td>
<td>5 V</td>
</tr>
<tr>
<td><strong>Input/output range</strong></td>
<td>0 ~ 5 V (100% of VDD)</td>
<td>0.5 ~ 4.5 V (80% of VDD)</td>
<td>0.05 ~ 3.25 V (97% of VDD)</td>
<td>0 ~ 5 V (100% of VDD)</td>
</tr>
<tr>
<td><strong>Quiescent current</strong></td>
<td>7.5 μA</td>
<td>2 μA</td>
<td>7.4 μA</td>
<td>NA</td>
</tr>
<tr>
<td><strong>DC gain</strong></td>
<td>82 dB</td>
<td>NA</td>
<td>65 dB</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Unity-gain frequency</strong></td>
<td>3.6 MHz for RL = 3.4 kΩ and C_L = 140 pF</td>
<td>NA</td>
<td>750 kHz</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Phase margin</strong></td>
<td>'109' (with R_D and 80’ (without R_D) for RL = 5.77 kΩ and C_L = 272 pF</td>
<td>47’ for RL = 577 Ω and C_L = 27.2 pF</td>
<td>50’ for C_C = 600 pF</td>
<td>&gt;45° for C_C = 100 pF~1000 pF</td>
</tr>
<tr>
<td><strong>Settling time</strong></td>
<td>3 μs (0.2 %) for RL = 3.4 kΩ and C_L = 140 pF</td>
<td>1.95 μs (±/− 10 mV) for RL = 10 kΩ and C_L = 24 pF</td>
<td>8 μs (0.2 %) for C_L = 600 pF</td>
<td>0.95 μs for C_L = 400 pF</td>
</tr>
<tr>
<td><strong>Offset voltage</strong></td>
<td>0.48 mV</td>
<td>NA</td>
<td>NA</td>
<td>6.1 mV</td>
</tr>
<tr>
<td><strong>Active area</strong></td>
<td>103×40 μm²</td>
<td>100×45 μm²</td>
<td>86×73.5 μm²</td>
<td>100×100 μm²</td>
</tr>
</tbody>
</table>

* indicates simulation results.


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