0.9 V rail-to-rail constant $g_{mn}$ CMOS amplifier input stage

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Presented is a 0.9 V rail-to-rail constant $g_{mn}$ CMOS amplifier input stage consisting of complementary differential pairs and a $g_{mn}$ control circuit. The $g_{mn}$ control circuit eliminates the $g_{mn}$ dead zone, which occurs in the conventional rail-to-rail amplifier with ultra-low supply voltages. The proposed amplifier input stage has a constant $g_{mn}$ that varies by $\pm 2.3\%$ for rail-to-rail input common-mode levels. To verify the proposed amplifier design, an experimental prototype operational amplifier is also implemented using 0.35 $\mu$m standard CMOS technology.

Introduction: The extensive usage of portable electronic products has created a large demand for low-supply voltage integrated circuits. This is particularly true for low-supply rail-to-rail CMOS operational amplifiers. However, many low-supply voltage applications require a rail-to-rail input stage to increase the signal-to-noise ratio. Fig. 1a shows a well-known method for obtaining a rail-to-rail input stage based on connecting $n$-channel and $p$-channel differential pairs in parallel. At least one of the two differential pairs is active for any input common-mode voltage ($V_{com}$). However, Fig. 1b shows that the transconductance ($g_{mn}$) of this input stage when both differential pairs are active (region II) is twice that of when only one pair is active (regions I and III). This large variation in $g_{mn}$ prevents optimal frequency compensation and introduces severe signal distortions. Researchers have proposed several methods to solve this problem [1, 2]. Recently, we proposed a 1 V rail-to-rail constant $g_{mn}$ scheme that keeps the sum of currents in the complementary differential pairs constant [3]. At ultra-low supply voltages, however, the sum of the common-mode voltage ranges of the $n$-channel and $p$-channel differential pairs may become larger than the available supply voltage. This creates a ‘dead zone’ in region II [2]. Fig. 1c shows that the dead zone produces a smaller value of total transconductance ($g_{mn}$). Our simulation result shows that the dead zone occurs when the supply voltage goes down below 1 V. This makes the conventional schemes not applicable to a 0.9 V opamp. To avoid generating a dead zone in the input range under ultra-low supply voltages, this Letter employs a negative feedback loop to keep the current of the differential pair close to the value of a reference level, which is set at the bottom of the dead zone.

Proposed circuit: The proposed amplifier input stage is operated in the weak inversion. The tail current of the $n$-channel differential pair depicted in Fig. 1a, can be obtained as

$$I_n \simeq 2I_{thn} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gn}}{n_n U_t} + \left( 2 \left( \frac{W}{L} \right) + \frac{W}{L} \right) \frac{V_{com} - V_{Gn}}{n_p U_t}$$

where $U_t$ is the thermal voltage, $I_{thn}$ is the zero bias current, $n$ is the sub-threshold slope coefficient, and ($W/L$)$_n$ and ($W/L$)$_p$ are the aspect ratios of the $n$-channel differential pair and the tail current device, respectively [4]. Neglecting the unity in the numerator of (1), the drain current of the differential pair in region III ($V_{com} > V_{Gn} + n_n U_t$) can be approximately expressed as:

$$I_{Dn} \approx \frac{I_n}{2} \simeq \frac{I_{thn}}{2} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gn}}{n_n U_t}$$

The transconductance is then described as

$$g_{mn} = \frac{I_{Dn}}{n_n U_t} \simeq \frac{I_n}{2n_n U_t} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gn}}{n_n U_t}$$  \hspace{1cm} (3)$$

Similarly, the transconductance of the $p$-channel differential pair in region I ($V_{com} < V_{Gp} - n_p U_t$) is then described as:

$$g_{mp} = \frac{I_{Dp}}{n_p U_t} \simeq \frac{I_n}{2n_p U_t} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gp}}{n_p U_t}$$  \hspace{1cm} (4)$$

For $V_{Gp} - n_p U_t < V_{com} < V_{Gn} + n_n U_t$, the drain currents of $n$- and $p$-channel pairs in region II can be approximately expressed as:

$$I_{Dn} = \frac{I_n}{2} \simeq \left( \frac{I_{thn}}{2} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gn}}{n_n U_t} \right)$$    \hspace{1cm} (5)$$

and

$$I_{Dp} = \frac{I_n}{2} \simeq \left( \frac{I_{thn}}{2} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gp}}{n_p U_t} \right)$$  \hspace{1cm} (6)$$

The $g_{mn}$ of the complementary differential pairs can then be described as

$$g_{mn} \simeq \frac{I_n}{n_n U_t} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gn}}{n_n U_t} + \frac{I_n}{n_p U_t} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gp}}{n_p U_t}$$  \hspace{1cm} (7)$$

Fig. 1b shows the transconductance of the proposed amplifier input stage when both differential pairs are active (region II) is twice that of when only one pair is active (regions I and III). This large variation in $g_{mn}$ prevents optimal frequency compensation and introduces severe signal distortions. Researchers have proposed several methods to solve this problem [1, 2]. Recently, we proposed a 1 V rail-to-rail constant $g_{mn}$ scheme that keeps the sum of currents in the complementary differential pairs constant [3]. At ultra-low supply voltages, however, the sum of the common-mode voltage ranges of the $n$-channel and $p$-channel differential pairs may become larger than the available supply voltage. This creates a ‘dead zone’ in region II [2]. The tail current transistors $g_{mn}$ is then described as

$$V_{Gn} \simeq \frac{V_{com}}{n_n U_t} + \frac{I_n}{n_n U_t} \left( \frac{W}{L} \right)$$

where $U_t$ is the thermal voltage, $I_{thn}$ is the zero bias current, $n$ is the sub-threshold slope coefficient, and ($W/L$)$_n$ and ($W/L$)$_p$ are the aspect ratios of the $n$-channel differential pair and the tail current device, respectively [4]. Neglecting the unity in the numerator of (1), the drain current of the differential pair in region III ($V_{com} > V_{Gn} + n_n U_t$) can be approximately expressed as:

$$I_{Dn} \approx \frac{I_n}{2} \simeq \frac{I_{thn}}{2} \left( \frac{W}{L} \right) \frac{V_{com} - V_{Gn}}{n_n U_t}$$

Substituting (8) into (5) and (6), the reference currents of the $n$- and $p$-channel pairs for achieving a constant $g_{mn}$ are:

$$I_{refn} \simeq 2I_{thn} \left( \frac{W}{L} \right) \exp \left( \frac{V_{com}}{n_n U_t} + \frac{n_n U_t}{n_n U_t} \ln \left[ \frac{n_n I_{thn}(W/L)_n}{n_p I_{thn}(W/L)_p} \right] \right)$$  \hspace{1cm} (9)$$

and

$$I_{refp} \simeq 2I_{thn} \left( \frac{W}{L} \right) \exp \left( \frac{V_{com}}{n_p U_t} - \frac{n_p U_t}{n_n U_t} \ln \left[ \frac{n_p I_{thn}(W/L)_p}{n_n I_{thn}(W/L)_n} \right] \right)$$  \hspace{1cm} (10)$$

Fig. 2 shows the simulated and calculated $g_{mn}$ against $V_{com}$ for different bias voltages of the tail current transistors.
Fig. 3 illustrates the proposed amplifier input stage, which consists of a complementary differential pair (M1–M6) and a \( g_m \) control circuit (M7–M12, \( R_{ref} \), single-stage differential amplifiers A1–A2, \( I_{refn} \) and \( I_{refp} \)). \( I_{refn} \) and \( I_{refp} \) are set according to (9) and (10). The amplifier, M7–M9, is a replica of the differential amplifier, M1–M3. Hence, the current in the devices of these two amplifiers is equal. A negative feedback loop consisting of A1, M7–M9, \( R_{ref} \), and \( I_{refn} \) maintains the tail current of the \( n \)-channel differential pair close to the value of \( I_{refn} \). A similar feedback loop keeps the currents in the \( p \)-channel pair at the value of \( I_{refp} \).

**Conclusion:** This Letter presents a 0.9 V rail-to-rail constant \( g_m \) CMOS amplifier input stage. The complementary differential pairs have a constant transconductance that varies by \( \pm 2.3\% \) for rail-to-rail input common-mode levels. Experimental results show that the proposed amplifier input stage is suitable for low-speed, low-power and ultra-low supply portable electronic products.

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14 July 2009
doi: 10.1049/el.2009.9033

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**References**


Fig. 3 Proposed ultra-low supply voltage rail-to-rail constant \( g_m \) amplifier input stage

**Simulation and experimental results:** The proposed amplifier was simulated and fabricated using 0.35 \( \mu \)m CMOS technology. Fig. 4 shows the simulated normalised amplifier transconductances against \( V_{com} \). Variations in \( g_m \) lie within an error interval of \( \pm 2.3\% \). The amplifier was connected as a unity gain closed-loop configuration and measured under a 25 pF capacitive load. A square wave input of a 0.9 V swing is applied to the input of the amplifier. The measured slew rates are 0.162 and 0.135 V/\( \mu \)s for the rising and falling edges, respectively. The total harmonic distortion (THD) with the input of a 0.9 V and 1 kHz sinusoidal input waveform is \(-59\) dB. The DC power consumption is 8 \( \mu \)W.

**Fig. 4** Simulated normalised transconductances against input common-mode voltage