A Low-Quiescent Current Two-Input/Output Buffer Amplifier for LCDs

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Abstract—This study proposes a low-quiescent current two-input/output buffer amplifier for LCD applications. A current reuse technique is employed in the output stage of the buffer amplifier to reduce the quiescent current consumption. An experimental prototype 6-bit LCD column driver with the proposed buffer amplifiers implemented in a 0.35-μm CMOS technology demonstrates that an average value of 0.6 μA static current is consumed in one channel driver. The settling time to settle within 0.2% of the final voltage is 6 μs under a 30-KΩ resistance and 30-pF-capacitance load. The area of this two-input/output buffer amplifier is 21.5 μm × 190 μm.

I. INTRODUCTION

With the increase in use of compact, light-weighted, low-power Liquid-Crystal Displays (LCDs), there is a large demand to develop a low-power dissipation LCD driver [1-2]. An LCD driver is generally composed of column drivers, gate drivers, a timing controller, and a reference source. The column drivers are especially important for achieving high-speed driving, high resolution, and low-power dissipation. A column driver generally includes registers, data latches, digital-to-analog converters (DACs) and output buffers. Among these, the output buffers determine the speed, resolution, and power dissipation of the column drivers [3-5]. Due to the hundreds of buffer amplifiers built into a single chip, the buffer amplifier should occupy a small die area, and its static power consumption should be small.

In order to improve the lifetime of the liquid crystal material, the liquid crystal of active matrix liquid crystal displays should be driven by a so-called inversion method, which alternates the positive and negative polarities between the liquid-crystal cell with respect to a common backside electrode. There are three inversion methods, which are frame, line and dot inversions for LCD driving. The dot inversion method is preferred in the high-resolution displays [6].

In the previous work [6], a rail-to-rail dot-inversion driving scheme, which utilizes two complementary differential amplifiers to drive a pair of column lines, was proposed. Figure 1 shows the driving method. Two channels of driving circuits, in which one channel takes the responsibility for driving negative polarity and the other for driving positive polarity, are grouped to drive a pair of adjacent column lines. PMOS input buffers are used to drive positive-to-negative polarity operation. NMOS input buffers are used for the transition of negative-to-positive polarity. The PMOS input buffers have a large discharge capability and vice versa for the NMOS input buffers. In this work, we combine these two buffers as a two-input/output buffer amplifier. A current reuse technique is employed in the proposed buffer amplifier to reduce the quiescent power consumption.

II. PROPOSED BUFFER AMPLIFIER

A. Analysis of a Typical Two-Stage Op Amp

A class-AB op amp is usually connected to a unity buffer for driving highly capacitive column lines of the display panel. Because the buffer amplifiers are required to have a high open-loop gain to obtain a low value of the systematic offset voltage, a two-stage amplifier is usually used in LCD drivers. A two-stage amplifier requires compensation for stability. Some buffer amplifiers adopt the output node as a dominant pole to achieve enough stability without a Miller capacitance [3, 6]. However, a charge conservation technique is commonly

Figure 1 A rail-to-rail dot-inversion driving scheme.
used in some LCD drivers to reduce the dynamic power dissipation [7]. Before a new scanning driving, all column lines are isolated from the buffers. Since the buffer amplifiers experience no load for a period of time, these amplifiers require the Miller compensation. Figure 2 shows an equivalent circuit of a typical two-stage op amp where \( g_{m1} \) and \( g_{m2} \) are the transconductances of the first and second stages, respectively; \( r_{o1} \) and \( r_{o2} \) are the output resistances of the first and second stages, respectively; \( C_{o1} \) and \( C_{o2} \) are the parasitic capacitances at output nodes of the first and second stages, respectively; \( C_C \) is the Miller compensation capacitor; and \( R_L \) and \( C_L \) are resistive and capacitive loads, respectively. The open-loop transfer function, \( A_o(s) \), can be obtained from Figure 2. That is:

\[
A_o(s) = \frac{A_{dc} \left( \frac{1}{\omega_{p1}} + s \right) \left( \frac{1}{\omega_{p2}} + s \right)}{\left( \frac{1}{\omega_{p3}} + s \right)} \tag{1}
\]

where

\[
A_{dc} = g_{m1}g_{m2}r_{o1}r_{o2} \tag{2}
\]

\[
\omega_{z1} = \frac{1}{C_L R_L} \tag{3}
\]

\[
\omega_{z2} = -\frac{g_{m2}}{C_C} \tag{4}
\]

\[
\omega_{p1} \equiv \frac{1}{r_{o1}r_{o2}g_{m2}C_C + C_L r_{o2}} \tag{5}
\]

\[
\omega_{p2} \equiv \frac{C_L g_{m2} + C_L / r_{o1}}{C_CC_L} \tag{6}
\]

\[
\omega_{p3} \equiv \frac{1}{(C_{o1} + C_{o2}) R_L} \tag{7}
\]

The unity gain frequency is

\[
\omega_t \equiv A_{dc} \omega_{p1} = \frac{g_{m1}g_{m2}}{C_L g_{m2} + C_L / r_{o1}} \tag{8}
\]

The larger ratio of \( g_{m2} \) over \( g_{m1} \), the larger the phase margin. If we want to achieve a phase margin of 75°, the value of \( g_{m2} \) should be 3.7 times of the value of \( g_{m1} \). Hence, the output stage of the buffer amplifier consumes more quiescent power than that of the first stage.

The zero of \( \omega_z \) is a negative value, so it can not compensate for the pole of \( \omega_{p2} \). Figure 3 shows the open-loop frequency characteristic of a two-stage op amp with/without \( C_L \) and \( R_L \) loads where the solid line and dashed line show the frequency characteristics with and without \( C_L \) and \( R_L \) loads, respectively. The phase margin of the op amp can be calculated from the equations below.

\[
\tan^{-1} \left( \frac{\omega_t}{\omega_z} \right) = 90° - PM \tag{14}
\]

\[
\frac{g_{m2}}{g_{m1}} = \frac{1}{\tan(90° - PM)} \tag{15}
\]

The zero of \( \omega_z \) is a negative value, so it can not compensate for the pole of \( \omega_{p2} \). Figure 3 shows the open-loop frequency characteristic of a two-stage op amp with/without \( C_L \) and \( R_L \) loads.
B. Proposed Two-Input/Output Buffer Amplifier

To reduce the quiescent power dissipation, we combine the NMOS input and PMOS input buffer amplifiers into a two-input/output buffer amplifier where a current reuse technique is employed in the output stage. Figure 4 shows the architecture of the proposed two-input/output buffer amplifier. It consists of an NMOS input and a PMOS input one-stage differential amplifiers, a complementary common source amplifier, M11-M12, and a floating bias circuit, \( I_{b1} \) and \( I_{b2} \), and M13-M16. Two outputs, out1 and out2, are isolated by M13 and M15. M13-M14 and M15-M16 form two floating current mirrors. The quiescent current, \( I_{11} \) and \( I_{12} \), of the complementary common source amplifier, M11-M12, is biased by the two floating current mirrors. That is:

\[
I_{11} = I_{12} = I_{b1} \left[ 1 + \left( \frac{W}{L} \right)_{13} + \left( \frac{W}{L} \right)_{15} \right] \quad (16)
\]

where \( I_{b1} = I_{b2} \). Although two additional bias currents, \( I_{b3} \) and \( I_{b4} \), are required, they consume smaller currents than that of the complementary common source amplifier. The output, out1, has a large charging capability and the output, out2, has a large discharging function. Hence, the proposed two-input/output buffer amplifier is suitable for the application in the LCD driver architecture of Figure 1.

![Figure 4 Architecture of the proposed two-input/output buffer amplifier.](image)

The circuit may suffer from a systematic output dc offset voltage. However, the dc offset voltage can be eliminated by sizing the transistors so as to satisfy the following constraint:

\[
\frac{I_{b3}}{2} \left( \frac{W}{L} \right)_{11} = \frac{I_{b4}}{2} \left( \frac{W}{L} \right)_{12} = I_{b1} \left[ 1 + \left( \frac{W}{L} \right)_{13} + \left( \frac{W}{L} \right)_{15} \right] \quad (17)
\]

where \( I_{b1} \) is the bias current for PMOS input one-stage differential amplifier.

Figure 5 shows the schematic of the proposed buffer amplifier. The NMOS input and PMOS input one-stage differential amplifiers are consisted of M1-M5 and M6-M10, respectively. The capacitors, \( C_{C1} = C_{C4} \) are the Miller compensation capacitors. In the stable state, the currents flowing in M9 and M10 are both \( I_{b3}/2 \) where \( I_{b3} \) is the bias current for NMOS input one-stage differential amplifier. The drain voltage of M10 equals to that of M9. The quiescent current of M11 is then mirrored from M9. Similarly, the quiescent current of M12 is mirrored from M4. Since the complementary common source amplifier is biased by the floating bias circuit and two one-stage differential amplifiers, the performance of the buffer amplifier compared with the state-of-the-art.

III. MEASUREMENT RESULTS

To verify the performance of the proposed buffer amplifier, a 6-bit 12-channel LCD column driver with the proposed buffer amplifiers was designed and was fabricated using a 0.35-μm CMOS technology. Figure 6 shows the die photograph. The area of one two-input/output buffer amplifier is 21.5 μm × 190 μm. The two-input/output buffer amplifier consumes 1.2-μA static current. This means that only 0.6-μA static current is consumed in one channel driver. Figure 7 shows the measured output waveform with a 30KΩ-resistance and 30pF-capacitance load when the digital data change from “000000” to “111111”. The settling time to settle within 0.2% of the final voltage is 6 μs. Figure 8 shows the measured results for DNL/INL in a linear 6 bit gray scale for 24 channels. The maximum DNL and INL are respectively measured as 0.024 LSB and 0.072 LSB with 1 LSB = 32 mV. Table 1 summarizes the performance of the buffer amplifier compared with the state-of-the-art.

![Figure 5 Schematic of the proposed buffer amplifier.](image)
This work presents a low-quiescent current two-input/output buffer amplifier. A current reuse technique is employed in the output stage of the buffer amplifier to reduce the quiescent current consumption. An experimental prototype 6-bit LCD column driver with the proposed buffer amplifiers was implemented in a 0.35-μm CMOS technology. The circuit draws an average value of 0.6 μA static current in one channel driver and exhibits the settling time of 6 μs for settling within 0.2 % of the final voltage under a 30 kΩ and a 30 pF capacitance loads. The measured data show that the proposed buffer amplifier is very suitable for dot-inversion LCD column drivers.

ACKNOWLEDGMENT
The authors would like to thank the Chip Implementation Center of the National Science Council for their support in chip fabrication.

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