A 9b Quasi-Pipeline DAC for Small-Format LCD Column Drivers

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Abstract

This paper proposes a 9b quasi-pipeline DACs and column multiplex techniques for small-format LCD column drivers. The DAC provides uniform channel performance, built-in gamma correction through nonlinear global resistor string values, and occupies a smaller column driver size. The maximum DNL and INL were measured as 0.25 LSB and 0.33 LSB, respectively. The averaged data conversion time is 16 ns per channel. The FoM of the proposed DAC is 0.2 pJ/bit/mm\textsuperscript{2}, which is smaller than that of prior arts.

1. Introduction

Achieving a higher color depth for LCD drivers requires a higher DAC resolution. To ensure channel uniformity, a resistor-string DAC (RDAC) is typically used for LCD column drivers [1]. However, the area of a high-resolution RDAC is prohibitively large, rendering it impractical for column drivers in high-color-depth displays [2]. To avoid this issue, prior arts proposed scalable DAC architectures with column multiplex techniques [3-4]. In this work, we propose a quasi-pipeline DAC with column multiplex techniques for LCD column driver applications.

2. Proposed Quasi-Pipeline DAC

Figure 1 shows the architecture of the proposed LCD column driver with quasi-pipeline DACs. A row of RDACs that shared the same global resistor string is used to convert the data with different intended resolutions for \(N\) column driving channels. Each column channel circuit contains a storage capacitor, a buffer, and a set of switches. To conduct the multiplex function, each channel requires its own storage capacitor. Since a large voltage swing on the storage capacitor can lead to extensive conversion time, we therefore adopt the pipeline operation to boost the conversion rate. The data conversion begins at the lowest resolution, \((n - n_1)\) bit, and ends at the highest resolution, \(n\) bit. Switches in the cross-link array are activated sequentially from the top to the bottom, and activated simultaneously from channel 1 to channel \(N\). While each RDAC converts data for the channel \(k\), the previous DAC begins the processing for channel \((k + 1)\). Consequently, the voltage swing on each of the storage capacitor is much reduced and results in much faster data conversion rate.

However, since the buffer amplifier must still drive a significant capacitive load, its output voltage may not properly track the storage capacitor voltage due to limited bandwidth. Additionally, the kickback noise would induce an error in the storage capacitor via the parasitic coupling between the buffer input/output, while the storage capacitor is isolated from the DAC after the data conversion. To solve this problem, we need to postpone the final data conversion by a few clock cycles. Until then, the voltage difference between the buffer input/output becomes negligible and so is the kickback noise.

3. Experimental Results

Using 0.35-\(\mu\)m CMOS technology, a 30-channel column driver with quasi-pipeline DACs is implemented. To demonstrate the data conversion linearity, the resistor values of the global resistor string are equalized. Figure 2 shows the die photo. Figure 3 shows the measured results of a linear 9b gray scale on six different chips. The maximum DNL and INL are measured as 0.25 LSB and 0.33 LSB, respectively, with 1LSB = 7 mV. The data conversion time for each of RDACs is 25 ns. The delay time between the first and the 29th driving channel outputs is 25 ns \times 28 = 700 ns. The time to settle within 0.2% of the final voltage is about 2 \(\mu\)s. Since we have set aside 80 clock cycles for delay lines, the data conversion time of the complete proposed DACs is estimated to be 25 ns \times (1,000/2 + 80 + 3) + 2 \(\mu\)s \(\equiv\) 16 \(\mu\)s for 1,000 channels. The averaged data conversion time is 16 ns per channel. Table 1 summarizes the performance. The FoM of the proposed DAC is 0.2 pJ/bit/mm\textsuperscript{2}, which is smaller than that of prior arts.

4. Summary

This works presents a 9b quasi-pipeline DAC and column multiplex techniques for small-format 16-million-color LCD column drivers. The maximum DNL and INL are measured as 0.25 LSB and 0.33 LSB, respectively, with 1LSB = 7 mV. The averaged data conversion time is 16 ns per channel. The measured results indicate that the
proposed 9b quasi-pipeline DAC is highly suitable for small-format 16-million-color LCD column driver ICs.

**Fig. 1 Architecture of the proposed LCD column driver with quasi-pipeline DACs.**

**Fig. 2 Die photo of 30-channel column driver with quasi-pipeline DACs.**

**Fig. 3 Measured DNL/INL from six separate chips.**

<table>
<thead>
<tr>
<th>CMOS Tech.</th>
<th>0.5 µm</th>
<th>0.35 µm/0.5 µm</th>
<th>0.35 µm/0.5 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>5V</td>
<td>5V/5.3V</td>
<td>3.3V/5V</td>
</tr>
<tr>
<td>Gray Scale</td>
<td>9b</td>
<td>10b</td>
<td>9b</td>
</tr>
<tr>
<td>DNL/INL[LSB]</td>
<td>0.1/0.7</td>
<td>0.1/0.4</td>
<td>0.25/0.33</td>
</tr>
<tr>
<td>Conversion rate</td>
<td>2 MSPS</td>
<td>13 MSPS</td>
<td>80 MSPS</td>
</tr>
<tr>
<td>Conversion time</td>
<td>500 ns</td>
<td>77 ns</td>
<td>16 ns/channel</td>
</tr>
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<td>Static Current Consumption</td>
<td>1 µA/DAC</td>
<td>250 µA/RDAC</td>
<td>600 µA/MDAC</td>
</tr>
<tr>
<td>Area</td>
<td>0.042mm²</td>
<td>0.238mm²/DA C</td>
<td>0.2×0.67×2mm² (DACs)</td>
</tr>
<tr>
<td>FoM</td>
<td>0.58</td>
<td>7.78</td>
<td>0.2</td>
</tr>
</tbody>
</table>

\[
FoM = \frac{T_c \cdot P}{N \cdot DACs / mm^2} = \frac{pJ}{b/mm^2} \quad [3]
\]

**Table 1 Performance summary.**

**References**