A Low Offset Buffer Amplifier for Liquid-Crystal Display Signal Driver

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ABSTRACT
An offset voltage adjustment technique, which can be used to reduce the offset voltage of the buffer amplifier in the liquid-crystal display signal driver, is proposed. This adjustment, which is finished before driving the display panel, does not need to be adjusted for every row scanning cycle and does not increase the settling time. An experimental prototype output buffer implemented in a 0.35-µm CMOS technology demonstrates that the circuit draws only 4.5 µA static current and exhibits the settling times of 5 µs for a voltage swing of 2.5 V under a 600 pF capacitance load with a power supply of 3.3 V. The offset voltage is reduced from 18 mV to 4 mV.

Keywords: offset voltage, adjustment technique, liquid-crystal display, signal driver.

INTRODUCTION
As Liquid-crystal displays (LCDs) are becoming larger and higher definition and an increasingly important concern with the advent of low-voltage design is the need for improved driving voltage range, there is a big demand of developing low-power dissipation, high-resolution, small settling time, high-speed and large output swing LCD driver [1-6]. An LCD driver is generally composed of column drivers, a controller, and a reference source. The column drivers are especially important to achieving high-speed driving, high resolution, low-power dissipation and large output swing [3-4]. Fig. 1 shows the block diagram of a column driver architecture. Digital display data are applied to the RGB inputs and sampled into the input register. A wide data latch presents one line of serially input pixel data to the inputs of digital-to-analog converters (DAC’s). In the DAC, a voltage level corresponding to a digital pixel data is appeared at its output. The output buffers, which are usually made of operational amplifiers, are used to drive highly capacitive column lines. The output buffers determine the speed, resolution, voltage swing and power dissipation of signal drivers [5].

The offset voltage is one of the most important specifications in the display driver system. A low offset buffer is needed to achieve a high quality and resolution display. Conventional offset-cancellation technique adds a holding capacitor to suppress the deviation [4]. Since this technique needs a cancellation period for every row scanning cycle, it causes a long time settling. In this work, an offset voltage adjustment technique is proposed to reduce the offset voltage of buffer amplifier. This adjustment is finished before driving the display panel. It does not need to be adjusted for every row driving. Hence, it will not increase the settling time.

OFFSET VOLTAGE ADJUSTMENT TECHNIQUE
Fig. 2 shows the configuration of the buffer amplifier in which a transistor-size adjustment is used to adjust the offset voltage. The offset adjustment is implemented by varying the sizes of the differential transistors. The adjustment flow is shown in Fig. 3. When the amplifier is under the adjustment, it is switched to an open loop and isolated from the output. A voltage of \( \frac{1}{2} V_{DD} \) is applied to both inputs of the amplifier. If the output voltage is high, increase the size of the inverting input transistor until the output voltage is decreased to a low value. Similarly, if the output voltage is low, increase the size of the other side transistor until the output voltage is increased to a high value. The increment of the transistor size can be implemented by paralleling some small transistors to the differential transistors. Fig. 4 shows the complete configuration of the proposed low offset buffer amplifier, where a delay chain is added in the circuit to control the size adjustment.

Figure 1 Block diagram of a column driver architecture.
transistor-size controller

Figure 2 Configuration of the buffer amplifier.

Open circuit

\[ V_{\text{out}} = V_{\text{in}} = \frac{1}{2} V_{\text{DD}} \]

increase non-inverting input transistor size

\[ V_{\text{in+}} \]

high

\[ V_{\text{in-}} \]

low

increase inverting input transistor size

Figure 3 Adjustment flow.

size adjustment

Figure 4 Complete configuration of the proposed low offset buffer amplifier.

Output Buffer

Fig. 5 shows the class-AB buffer circuit. As a buffer, out1 is connected to the inverting input (in-) and the input signal is applied to the non-inverting terminal (in+). The differential pair M6-M7, which is biased by the constant current source M1-M5, is actively loaded by the current mirror formed by M8 and M9. M10 – M13 are two sets of comparators, which are used to sense and amplify the voltage difference of the two inputs. Then the outputs of the comparators turn on/off the output stage (M14 – M17). The aspect ratio of M10 is chosen to be a little bit smaller than half of M5 but the W/L of M11 is designed to be a little bit larger than that of M9. Similarly, the aspect ratio of M12 is chosen to be a little bit larger than half of M5 but the W/L of M13 is designed to be a little bit smaller than that of M9, i.e.,

\[
\frac{W}{L}_{10} = \frac{1}{2} \frac{W}{L}_{5} - \Delta \frac{W}{L} \\
\frac{W}{L}_{11} = \frac{W}{L}_{9} + \Delta \frac{W}{L} \\
\frac{W}{L}_{12} = \frac{1}{2} \frac{W}{L}_{5} + \Delta \frac{W}{L} \\
\frac{W}{L}_{13} = \frac{W}{L}_{9} - \Delta \frac{W}{L}
\]

In the stable state with no input, the output voltage equals to the input voltage. The currents flowing in M6 - M7 are all \( I/2 \). Since the aspect ratio of M10 is designed to be smaller than half of M5 and the W/L of M11 is designed to be larger than that of M9, this will make M11 be in the triode region. As a result, the gate voltages of M15 and M17 will be forced to be close to the value of \( V_{SS} \). M15 and M17 will then stay at “off”. Similarly, the output transistors M14 and M16 will also be cut off from the output in the stable state.

Figure 5 Buffer amplifier.

When the input voltage of the non-inverting terminal is increased, the output voltage of the differential pair will be increased. Then the output transistors M15 and M17 will still stay in the cut off region but M14 and M16 will be turned on to charge the output node. The gate voltages of M14 and M16 can be pulled down to very low levels, so they can charge the output load at a maximal speed. Similarly, when the input voltage of the non-inverting terminal is reduced, M15 and M17 will discharge the output node.

Experimental Results

The output buffer amplifiers with and without offset adjustment were fabricated using a 0.35-µm CMOS...
technology. Their die photographs are shown in Fig. 6 and 7, respectively. The die areas of the buffer with and without offset adjustment are $44.7 \times 69 \ \mu\text{m}^2$ and $210 \times 69 \ \mu\text{m}^2$, respectively. Most of the die area is the delay chain. Since the delay chain can be applied to all of the buffers in the signal driver, the overhead is very small for a whole driver chip. A quiescent current consumption of 4.5 µA is measured at a power supply of 3.3 V. Fig. 8 shows the measured results of the step response of the proposed buffer amplifier loaded with a large size capacitor of 600 pF before the offset adjustment. The upper trace is the input waveform and the lower one is the measured output waveform. The setting time for the output to settle to within ±5 mV of the final voltage is only 5 µs. Fig. 9 shows the voltage difference between the input and output nodes. It can be seen that the maximum offset voltage is 18 mV. Figs 10 and 11 show the same measurement on the proposed low offset buffer amplifier. They can be seen that the settling time is unchanged but the offset voltage is reduced to 4 mV.

Conclusions
In this work, an offset voltage adjustment technique, which can be used to reduce the offset voltage of the buffer amplifier in the liquid-crystal display signal driver, has been presented. Since the adjustment is finished before driving the display panel, it does not increase the settling time. An experimental prototype output buffer implemented in a 0.35-µm CMOS technology demonstrates that the circuit draws only 4.5 µA static current and exhibits the settling times of 5 µs for a voltage swing of 2.5 V under a 600 pF capacitance load with a power supply of 3.3 V. The offset voltage is reduced from 18 mV to 4 mV. The measured data do show that the proposed low offset buffer amplifier is suitable for the LCD signal driver.
Figure 10 Measured step response after the offset adjustment.

![Figure 10](image)

Figure 11 Voltage difference between the output and input nodes after the offset adjustment.

![Figure 11](image)

REFERENCES


