56.3: A High-Speed Low-Power Rail-to-Rail Buffer Amplifier for LCD Driver Application

Chih-Wen Lu
Department of Electrical Engineering, National Chi Nan University

Abstract
A high-speed low-power rail-to-rail buffer amplifier, which is suitable for liquid crystal display driver application, is proposed. The buffer draws little current while static but has a large driving capability while transient. The circuit achieves the low dc power consumption but large driving capability by employing the variable-gain amplifiers to sense the transients of the input to turn on the output transistors, which are statically off in the stable state. This increases the speed of the circuit without increasing static power consumption too much. An experimental prototype output buffer implemented in a 0.35-μm CMOS technology demonstrates that the circuit can operate under a wide power supply range. Quiescent current of 5 μA is measured. The buffer exhibits the settling times of 1.5 μs for a voltage swing of 0.1 ~ (VDD – 0.1) V under a 600 pF capacitance load. The area of this buffer is 30×98μm².

1. Introduction
As Liquid-Crystal Displays (LCDs) are recently installed in notebook type personal computers and compact desktop personal computers and monitors are becoming larger and higher definition, there is a large demand of developing low-power dissipation, high resolution, small settling time and high-speed LCD driver [1-6]. An LCD driver is generally composed of column drivers, gate drivers, a timing controller, and a reference source. The column drivers are especially important to achieving high-speed driving, high resolution and low-power dissipation [1-3]. A column driver generally includes registers, data latches, digital-to-analog converters (DAC’s) and output buffers. Among those, the output buffers determine the speed, resolution, voltage swing and power dissipation of the column drivers [2, 5]. Due to thousands of output buffer amplifiers built into a single chip, the buffer should occupy a small die area, and its static power consumption should be small. The output buffer should offer an almost rail-to-rail voltage driving which can accommodate higher gray levels. Also, the settling time should be smaller than the horizontal scanning time.

Some output buffers were proposed and demonstrated to reduce the power consumption in recent years. For examples, Yu et al [4] proposed a class-B output buffer for flat-panel-display column driver, for which a comparator was used in the negative feedback path to eliminate the quiescent current in the output stage. Weng et al. [5] proposed a compact, low-power, and rail-to-rail class-B output buffer for driving the large column line capacitance of LCDs, where a nonlinear element in feedback path is modified from the current-mirror amplifier to obtain the area and power advantages. Lu [2] proposed a high-speed driving scheme and a compact high-speed low-power rail-to-rail class-B buffer amplifier, which are suitable for both of the small- and large-size liquid crystal display applications. This buffer amplifier employs a double cascade current mirror as the load of the rail-to-rail differential pairs. Since the cascade current mirror is a self-bias configuration, it cannot be operated under a wide range of power supply. An LCD driver should be applicable to different power supplies [7]. In this work, a high-speed low-power rail-to-rail buffer amplifier, which can be operated under a wide range of power supply, is proposed.

2. Proposed Buffer Amplifier
The architecture of the proposed buffer amplifier is shown in Figure 1, which is composed of three stages. The first stage is a rail-to-rail differential amplifier. The second stage is a variable-gain amplifier. In order to drive the large capacitive load of the LCD panel, the complementary push-pull transistors are used as the last stage. The bias of the push-pull transistors should be carefully designed. Otherwise, it will consume large dc current. This is very critical for the LCD driver. In this work, these two variable-gain amplifiers are used to control the current of the output stage. In the stable state, the gains of the amplifiers are too small to activate the output stage. The dc current of the output stage is then very small. However, during the transient, the gains of these two amplifiers are raised up to conduct the output stage. The output stage then drives the output load.

![Variable gain](image)

**Figure 1** The architecture of the proposed buffer amplifier.

Based on the architecture of the proposed buffer amplifier, a schematic of rail-to-rail buffer amplifier is designed and shown in Figure 2. The connected points are labeled with the alphabets A ~ H. As a buffer, “output” is connected to the inverting input (in-) and the input signal is applied to the non-inverting terminal (in+). The capacitive load is connected to the output. This buffer consists of a bias stage (Mb1~Mb8 and Rb), a rail-to-rail differential amplifier (M1~M20), two complementary common-source amplifiers as the second stage (M21~M26), and the complementary push-pull transistors (M27 and M28). The rail-to-rail differential pairs M3~M4 and M7~M8, which are biased by the constant current sources M1~M2 and M5~M6, are actively loaded by the current mirrors (M13~M20). The current mirrors, which are biased by the constant current sources (M9~M12) to
applicable different supply voltages, are also used to add and amplify two input signals of the differential pairs. The amplifiers of the second stage, whose gains are variable, are used to further amplify the input signals and control the current of the output transistors.

![Figure 2 The schematic of the proposed rail-to-rail buffer amplifier.](image)

The variable-gain amplifiers are implemented by the complementary common-source amplifiers, in which one amplifier is degenerated. M21 and M22 are two complementary common-source amplifiers but M22 is degenerated by M23. M23 is operated in the triode region and is controlled by the output of the cascode current mirrors (M13–M20). In the stable state, the drain voltages of M14 and M20 are equal to those of M13 and M19, respectively. The current in the current mirror is mirrored to the transistors of the second stage. Since M22 is degenerated, M21 stays in the triode region. The gain of this complementary is then small in the stable state. Also, the drain voltage of M21 is forced to near VDD. Similarly, for the complementary common-source amplifiers M25 and M26, the gain is small and the drain voltage of M26 is near to ground. This makes the output transistors M27 and M28 cut off from the output node and consume no power in the stable state.

When the input voltage, \( \text{in}^+ \), is reduced, the currents in M3 and M8 will be increased, but the currents in M4 and M7 will be decreased. The gate voltages of M14 and M20 will be increased and the gate voltages of M21–M26 will be decreased. As a result, M26 will go into the saturation region. The drain voltage of M26 will increase to turn on M28. Then M28 starts to discharge the output node. However, M27 is still in the cut off region. When the output voltage reaches the level that the voltage difference between the input and output is almost zero, M28 stops discharging the output node. Since the gate voltage of M28 can reach a value of VDD, M28 can be turned to fully “on” to discharge the output at a maximal speed. Similarly, when the input voltage, \( \text{in}^+ \), is increased, M28 is still cut off from the output, but the gate voltage of M27 is reduced and M27 starts to charge the output load until the output voltage almost equal to the input voltage. The gate voltage of M27 can be pulled down to a very low level, so M27 can charge the output load at a maximal speed.

3. Experimental Results

The proposed output buffer amplifier was fabricated using a 0.35-\( \mu \)m CMOS technology, in which the breakdown voltage is 8 V. The die photograph is shown in Figure 3. Since the proposed circuit is rather neat, the area of the buffer is only 30 x 98 \( \mu \)m².

Quiescent current of 5 \( \mu \)A of one buffer is measured. The column line of the LCD panel is a resistance and capacitance distribution. In this work, a 5 order RC configuration, which is shown in Figure 4, is used for the measurement. The resistance value is 2 k\( \Omega \) and the capacitance is 20 pF. The maximum settling time is located at the end point. Hence, this point is measured in this work. Figures 5 and 6 show the measured results of the output with the input of a large dynamic range (0.1 ~ 7.9 V and 0.1 ~ 3.2 V, respectively) of a 20 KHz triangular wave of the proposed buffer amplifier under the power supplies of 8 V and 3.3 V, respectively. The upper traces are the input waveforms and the lower ones are the measured output waveforms. They can be seen that the outputs basically follow the inputs for a almost full swing. Hence, the proposed buffer amplifier can be operated under a wide range of power supply. The step response of the same buffer with the voltage swing of 100 mV under power supply of 8 V is shown in Figure 7. It can be seen that the buffer is stable. Figures 5 and 6 show the measured results of the output with the input of a large dynamic range (0.1 ~ 7.9 V and 0.1 ~ 3.2 V) of a 50 KHz square wave of the proposed buffer amplifier under the power supplies of 8 V and 3.3 V, respectively. The settling times for the output to settle to within ±5 mV of the final voltage are 4 \( \mu \)s. Some conventional LCD buffer amplifiers used a large capacitor as the load. In order to compare the performances with the previous buffer amplifiers, a large capacitance of 600 pF is also used as the load for the measurements. Figure 10 shows the measured step response with the input of a large dynamic range (0.1 ~ 7.9 V) of the proposed buffer amplifier under a power supply of 8 V. The settling time is only 1.5 \( \mu \)s. The performance of the proposed buffer is summarized in Table 1. Compared with the previous buffers, the proposed circuit is superior in power supply range, input/output voltage range, area, quiescent power consumption and settling time.

![Figure 3 Die photograph of the proposed buffer amplifier.](image)
Figure 4 Equivalent circuit of the driven line.

Figure 5 The measured result of the output with the input of a large dynamic range (0.1 ~ 7.9 V) of a 20 KHz triangular wave of the proposed buffer amplifier under a 8-V power supply.

Figure 6 The measured result of the output with the input of a large dynamic range (0.1 ~ 3.2 V) of a 20 KHz triangular wave of the proposed buffer amplifier under a 3.3-V power supply.

Figure 7 The step responses of the buffer amplifier with the voltage swing of 100 mV.

Figure 8 The step response with the voltage swing of 0.1 V ~ 7.9 V under a 5 order RC load and 8-V power supply.

Figure 9 The step response with the voltage swing of 0.1 V ~ 3.2 V under a 5 order RC load and 3.3-V power supply.
Table 1 Performance Summary

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Process technology</td>
<td>0.35 μm CMOS</td>
<td>0.35 μm CMOS</td>
<td>0.8 μm CMOS</td>
<td>0.35 μm CMOS</td>
</tr>
<tr>
<td>VDD (V)</td>
<td>3.3 ~ 8</td>
<td>3.3</td>
<td>5</td>
<td>3.3</td>
</tr>
<tr>
<td>Input/output range (V)</td>
<td>0.1 ~ (VDD – 0.1)</td>
<td>0.05 ~ 3.25</td>
<td>1 ~ 5</td>
<td>0 ~ 3.3</td>
</tr>
<tr>
<td>Quiescent current (μA)</td>
<td>5</td>
<td>7.4</td>
<td>24</td>
<td>?</td>
</tr>
<tr>
<td>Settling time (μs)</td>
<td>1.5 for C_L = 600 pF</td>
<td>8 for C_L = 600 pF</td>
<td>8 for C_L = 600 pF</td>
<td>2.4 for C_L = 600 pF</td>
</tr>
<tr>
<td>Area (μm²)</td>
<td>30×98</td>
<td>86×73.5</td>
<td>230×140</td>
<td>46.5×57</td>
</tr>
</tbody>
</table>

4. Conclusions
In this work, a high-speed low-power rail-to-rail buffer amplifier, which is suitable for LCD driver applications, is proposed. An experimental prototype output buffer implemented in a 0.35-μm CMOS technology demonstrates that the circuit can operate under a wide power supply range of 3.3 ~ 8 V. If the buffer amplifier is fabricated in a high voltage technology, it can be operated at a higher supply voltage. Quiescent current of 5 μA of one buffer is measured. The buffer exhibits the settling time of 1.5 μs for a voltage swing of 0.1 ~ 7.9 V under a 600 pF capacitance load with the power supply of 8 V. The area of this buffer is $30 \times 98 \mu \text{m}^2$. Compared with the previous buffers, the performance of the proposed circuit is superior in power supply range, input/output voltage range, area, quiescent power consumption and settling time. The measured data do show that the proposed output buffer amplifier is very suitable for LCD driver applications.

5. Acknowledgements
The author would like to thank the Chip Implementation Center of National Science Council for their support in chip fabrication.

6. References