Abstract—A high-driving class-AB buffer amplifier, which consists of a high-gain input stage and a pseudo source follower, is proposed. The pseudo source follower consists of two same types of differential pairs rather than two complementary error amplifiers. The high-driving capability is mainly provided by the folded amplifiers. An experimental prototype buffer amplifier implemented in a 0.35-μm CMOS technology demonstrates that the circuit dissipates an average static power consumption of only 660 μW at a power supply of 3.3 V, and exhibits the slew rates of 2.7 V/μs and 3.8 V/μs for the rising and falling edges, respectively, under a 300Ω/150 pF load. The second and third harmonic distortions (HD2 and HD3) are -67 dB and -65 dB, respectively, at 20 KHz under the same load.

Index Terms—class-AB, buffer amplifier, pseudo source follower, error amplifier.

I. INTRODUCTION

The class-AB buffer amplifier is widely used for driving heavy resistive or capacitive loads [1-5]. To achieve the extended voltage swing, the output transistors should be connected in a common-source configuration. The quiescent current of the output transistors should be small, while the dynamic current should be as large as possible. The gates of the two output transistors are normally driven by two in-phase ac signals separated by a dc voltage. For example, Hogervorst et al. [4-5] proposed a two-stage, compact, power-efficient 3 V CMOS operational amplifier, in which the output stage is biased by a floating class-AB control. Langen et al. [6] also proposed compact low-voltage power-efficient operational amplifier cells for VLSI, in which a class-AB control is used to bias the output transistors. The above amplifiers are compact and power-efficient. Another approach, which employs a pseudo source follower shown in Fig. 1 to realize class-AB CMOS buffer amplifiers, have been widely used for a large voltage swing output. It is composed of a pair of complementary common-source transistors with two feedback loops consisting of a pair of complementary error amplifiers [7-10]. This offers a wide output voltage swing and a large ratio between the maximum transient current (class B current) and the quiescent current. However, when the input voltage of the pseudo source follower is near to VDD/VSS, the gate-to-source voltage of the output transistors cannot reach a large value [5]. Fig. 2 shows the schematic of the conventional pseudo source follower. When the input voltage is near to VSS, the maximum gate-to-source voltage of M12 is only \( V_{SGS} - V_{SDS} \) where \( V_{SGS} \) and \( V_{SDS} \) are the source-to-gate and source-to-drain voltages of M8, respectively. This limits the drive capability of the pseudo source follower. Also, the NMOS input error amplifier (M1–M5) conducts no current for a low level input. Then the node at the gate of M11 is high impedance and is easy to be disturbed. In this work, a new pseudo source follower is proposed to overcome this problem. The pseudo source follower employs two same types of error amplifiers rather than the complementary ones. Each error amplifier uses a folded amplifier to obtain a driving capability. The proposed buffer amplifier is designed to work at voice band frequencies for the telecommunication and audio applications.

Fig. 1 The conventional architecture of class-AB buffer amplifier.

II. PROPOSED CLASS-AB BUFFER AMPLIFIER

The proposed class-AB buffer amplifier has the same architecture in Fig. 1 but its pseudo source follower employs two same types of differential pairs. Fig. 3 shows the first error amplifier, A1, which drives the output PMOS transistor, M23. This error amplifier, which is consisted of M1–M9, is a folded amplifier. M2 and M3, which are biased by M1, form the input differential pair. The active load, M4 and M5, is folded by the constant current sources, M8 and M9. M6-M7 are two common-gate amplifiers. When the voltage of the inverting input terminal, in1–, is increased, the current flowing in M3 is reduced but the current in M5 is increased. Then the gate voltage of the PMOS output transistor, M23, is pulled down to a lower level, so M23 starts to charge the output node.
Since the gate voltage of M23 can be pulled down to minimum level of $V_{DS7(\text{triode})} + V_{DS9(\text{triode})}$, which is very close to VSS, M23 has a large driving capability.

The second error amplifier, A2, is shown in Fig. 4. The differential pair is biased by M10 and its currents are mirrored to the folded active load by the current mirrors of M13-M16. M21-M22 are the folded active load of the differential pair. When the voltage of the inverting input terminal is reduced, the currents in M12, M14, and M15 are increased. However, the current flowing in M21 is reduced. This increases the gate voltage of the output NMOS transistor, M24. M24 then discharges the output node. Since the gate voltage of M24 can be raised up to a maximum value of $V_{DD} - (V_{SD18(\text{triode})} + V_{SD20(\text{triode})})$, which is very close to VDD, M24 has a large discharge capability. This means that the proposed pseudo source follower has a large driving capability.

Fig. 2 The schematic of the conventional pseudo source follower.

Fig. 3 The proposed first error amplifier, A1.

Fig. 4 The proposed second error amplifier, A2.

Fig. 5 shows the complete schematic of the proposed class-AB buffer amplifier where M25-M31 consists of a two-stage amplifier, M1-M9 and M10-M22 form the first and second error amplifier, respectively, and M23-M24 are two output transistors. The resistors of Rcs1-Rcs3 and capacitors of Ccs1-Ccs3 are used for the Miller compensation. Since all of the differential pairs are the same types, they have the same input common-mode range. When the input voltage is near to VSS, the gate voltage of M23 is still well controlled. This overcomes the above problem of the conventional circuit.
III. EXPERIMENTAL RESULTS

The proposed output buffer amplifier was fabricated using a 0.35-μm CMOS technology. The die photograph is shown in Fig. 6. The active area of the buffer is only 242 × 47 μm². Fig. 7 shows the measured result of the output with the input of 2.4 V swing of a 20 KHz triangular wave of the unity-gain buffer amplifier loaded with 300 Ω resistor in parallel with a 150 pF capacitor. It can be seen that the output basically follows the input. The step responses of the unity-gain buffer amplifier with the same load with the voltage swings of 20 mV and 2.4 V are shown in Fig’s. 8 and 9, in which Fig. 8 shows the small signal response with 20 mVpp and Fig. 9 shows the large signal response with 2.4 Vpp. The slew rates are 2.7 V/μs and 3.8 V/μs for the rising and falling edges, respectively. Fig. 10 shows the measured results of the output with the input of a large dynamic range (2.4 Vp-p) of a 20 KHz sinusoidal wave for the unity-gain buffer amplifier. Fig. 11 shows its magnitude spectrum of the proposed buffer amplifier with a 2.4 Vp-p output swing into a 300Ω/150pF load. The second and third harmonic distortions (HD2 and HD3) are -67 dB and -65 dB, respectively, at 20 KHz under the same load. All of the measured results are summarized in Table 1.

IV. CONCLUSION

A high-driving class-AB buffer amplifier, which employs two pseudo source followers, has been presented. An experimental prototype buffer amplifier implemented in a 0.35-μm CMOS technology demonstrates that the circuit dissipates an average static power consumption of only 660 μW at a power supply of 3.3 V, and exhibits the slew rates of 2.7 V/μs and 3.8 V/μs for the rising and falling edges, respectively, under a 300Ω/150 pF load. The second and third harmonic distortions (HD2 and HD3) are -67 dB and -65 dB, respectively, at 20 KHz under the same load.
capacitor.

Fig. 8 The measured step response of the unity-gain buffer amplifier loaded with 300 Ω resistor in parallel with a 150 pF capacitor with the voltage swing of 20 mV.

Fig. 9 The measured step response of the unity-gain buffer amplifier loaded with 300 Ω resistor in parallel with a 150 pF capacitor with the voltage swing of 2.4 V.

Fig. 10 The measured results of the output with the input of a large dynamic range (2.4 Vp-p) of a 20 KHz sinusoidal wave for the unity-gain buffer amplifier.

Fig. 11 The measured magnitude spectrum of the proposed buffer amplifier with a 2.4 Vp-p output swing into a 300Ω/150pF load.

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REFERENCES

Table 1 Performance summary.

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<td>Technology</td>
<td>0.35-μm 1P4M CMOS</td>
<td>Proprietary P2 CMOS</td>
<td>5-μm CMOS</td>
<td>1.2-μm 2P2M CMOS</td>
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<tr>
<td>Die area</td>
<td>242 x 47 μm² (active)</td>
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<td>3.3 V ± 5 V</td>
<td>± 5 V</td>
<td>± 5 V</td>
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<td>Open loop gain</td>
<td>85 dB</td>
<td>83 dB</td>
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<td>Slew rate (rise)</td>
<td>2.7 V/μs</td>
<td>0.6 V/μs</td>
<td>1.5 V/μs</td>
<td>0.65 V/μs</td>
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<tr>
<td>Slew rate (fall)</td>
<td>3.8 V/μs</td>
<td>(freq. = 20 KHz, Vout,pp = 2.4 V, RL = 300 Ω, CL = 150 pF)</td>
<td>(freq. = 4 KHz, VIN = 3.3 V, RL = 300 Ω, CL = 1000 pF)</td>
<td>(freq. = 3 KHz, VIN = 3 V, RL = 200 Ω)</td>
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<td>Harmonic distortion</td>
<td>THD = -67 dB</td>
<td>(HD2 = -67 dB, HD3 = -65 dB)</td>
<td>HD2 = -73 dB</td>
<td>HD3 = -78 dB</td>
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<td>Input common mode range</td>
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<td>Power dissipation</td>
<td>660 μW</td>
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