P-57: A 10-Bit TFT-LCD Column Driver with Hybrid Digital to Analog Converters

Chih-Wen Lu and Zhi-Yu Xu
Department of Electrical Engineering, National Chi Nan University
1, University Rd, Pulii, Nantou Hsien, Taiwan, R.O.C.

Abstract
A 10-bit TFT-LCD column driver with hybrid DACs is proposed. The data conversion is implemented by an R-DAC and a C-DAC, which are used for the MSB and LSB data conversions, respectively. The simulated results show that the DAC exhibits the maximum DNL and INL of 0.28 LSB and 0.35 LSB, respectively. The settling time is within 4 μs. The areas for one R-DAC and one C-DAC are 0.438 × 1.063 mm² and 0.207 × 0.11 mm², respectively.

1. Introduction
As Thin-Film Transistor Liquid-Crystal Displays (TFT-LCDs) are installed in high definition monitors and televisions, there is a large demand for developing a high resolution and high color depth driver IC [1-3]. For example, an LCD-TV needs 2¹⁰×³ (1,073,741,824) colors [2-3]. In order to develop a high-quality display module, the driver system should be promoted to a higher level. An LCD driver system is generally composed of column drivers, row drivers, a timing controller, and a reference source. The column drivers are especially critical for achieving high-quality displays [1, 4-5]. For LCD-TV applications, they should process 10-bit digital input codes and then convert the input codes to analog levels.

A column driver generally includes shift registers, input registers, data latches, level shifters, Digital to Analog Converters (DACs) and output buffers [1, 5-6]. Among those, the DACs occupy the largest area. Due to hundreds of channels built into a single chip, the area of DACs should be reduced especially for the high color depth displays. Bell proposed an LCD column driver using a linear switch capacitor DAC [2-3]. The compensation of the nonlinear LC characteristic is made by the timing controller. The die area is largely reduced. We also proposed a 10-bit LCD column driver, in which piecewise linear digital to analog converters are utilized for each channel to reduce the die area [7]. The piecewise linear DAC is composed of an R-ladder type DAC (R-DAC) and a charge sharing DAC. However, the charge sharing DAC used eight units of capacitors. In this work, to further reduce the die area, a cyclic DAC (C-DAC), which uses two units of capacitors only, is utilized in the column driver.

2. Proposed Data Converter
In this work, a hybrid DAC, which consists of a 6-bit R-DAC and a 4-bit C-DAC, are utilized in the proposed column driver to reduce the die area and increase the resolution for a higher color depth display. A TFT-LCD driver IC should supply both positive and negative polarity voltages for the same digital input. Hence, 124 reference voltages are needed for the 6-bit R-DAC. A resistor string is used to generate these 124 reference voltages. The gamma voltages are applied to the resistor string and the resistor values can be made unequal to compensate for the nonlinear LC characteristic. The coarse gamma correction is made by the external reference voltages and the fine compensation is adjusted by a simple digital circuit, which can be built in the timing controller or the column driver. The characteristic of the C-DAC is linear. Hence, the characteristic of the hybrid DAC is piecewise linear.

Since the column driver IC should drive the LCD with positive and negative polarities, the DACs and output buffers are classified into positive and negative components. Figure 1 shows the data conversion scheme. Each channel contains one 6-bit R-DAC decoder, one 4-bit C-DAC and one buffer. Two neighboring channels, in which one channel is responsible for driving positive polarity and the other for driving negative polarity, are grouped and take turns to drive a pair of adjacent data lines of the LCD panel. The odd DACs and buffers are designed to be used for the negative polarity operation while the positive polarity operation is driven by the even DACs and buffers. When the odd column lines are under negative polarity and the even column lines are under positive polarity, the input codes and the output buffers are in a normal order. However, when the polarities of the column lines are exchanged, i.e., the odd and even column lines are alternated to positive and negative polarities, respectively, the orders of the input codes, DACs, and output buffers are exchanged. The odd DACs still take responsibility for negative polarity operation and vice versa for the even DACs.

The data conversion is serially implemented by the R-DAC and C-DAC. The decoder for the R-DAC selects two neighboring voltages from the resistor string according to the 6 most significant bits (MSBs) and sends them to the C-DAC. Then the C-DAC uses the two neighboring voltages to do the voltage division based on the 4 Least Significant Bits (LSBs) and passes the final voltage to the buffer. The schematic of the R-DAC is similar to our previous work [7].

The C-DAC, as shown in Figure 2, consists of a parallel-to-serial converter, four switches and two capacitors. The two capacitors have the same value. The digital data are serially applied to the switches, SW1 and SW2. The conversion is performed one bit at a time, resulting in 4 cycles required for each conversion. Each cycle contains sample and redistribution operations. For the first cycle, \( V_i \) is sampled to C2. At the same time, \( V_i \) or \( V_{i+1} \), which depends on the input bit, is read to C1. Then the voltages of C1 and C2 are averaged by turning on SW4. For the other three cycles, a new voltage (\( V_i \) or \( V_{i+1} \)) is read to C1. Then SW4 performs the average operation for the voltages of C1 and C2. The output voltage at the end of the fourth cycle of the conversion can be written as

\[
V_{out} = V_i + \sum_{k=0}^{124} \left( b_k V_{i+k} + b_{k+1} V_{i+k+1} \right) \frac{-V_i}{2} \]  

(1)
3. Proposed Column Driver Architecture

Based on the above data conversion scheme, the block diagram of the LCD column driver is shown in Figure 3, which consists of an inversion controller, shift registers, input registers, data latches, level shifters, 6-bit R-DACs, 4-bit C-DACs and output buffers. Digital display data are applied to input registers through the inversion controller. Some of the input data will be inverted for the TFT-LCD inversion operation by this inversion controller. A wide data latch presents one row of serial input pixel data to the level shifters. Then the voltage level of the digital signals is boosted to a higher level by these level shifters. In the DAC, a voltage level corresponding to a digital pixel data appears at its output. Here, the data conversion is implemented by R-DACs and C-DACs in series. The output buffers, in which the schematic is similar to our previous work [7], are used to drive highly capacitive column lines.

4. Simulated Results

A 10-bit LCD column driver with the proposed hybrid DACs was simulated using a 0.35-μm 5-V CMOS technology. Figure 4 shows the 4-channel layout. The resistor string is put in the middle of the layout. The DACs and output buffers are located at the two sides. The areas for one R-DAC and one C-DAC are 0.438 × 1.063 mm² and 0.207 × 0.11 mm² respectively.

The Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) are usually measured for a DAC. However, it is difficult to show these two specifications for a nonlinear DAC. In order to demonstrate the performance of the proposed circuit, the nonlinear Gamma voltages are not applied to the resistor string and the resistor values are made up equal. Figs. 5 (a) and (b) show the values of DNL for positive and negative polarities, respectively, while the values of INL are shown in Figs. 6 (a) and (b) for positive and negative polarities, respectively. The maximum DNL and INL are 0.28 LSB and 0.35 LSB, respectively. The simulated output waveforms of three neighboring channels under dot inversion and the load resistor of 5 kΩ and capacitor of 150 pF for the RGB digital inputs of...
‘1111111111’ are shown in Figure 7, in which the voltage levels for negative and positive polarities are 4.83 V and 0.17 V, respectively. From this figure, it can be seen that the settling time is within 4 μs. Table 1 shows the performance summary.

5. Conclusion

A 10-bit LCD column driver with hybrid DACs has been presented. The hybrid DAC is decomposed of a 6-bit R-DAC and a 4-bit C-DAC to reduce the die area. The coarse Gamma correction is made by the external reference voltages and the unequal resistor values of the resistor string. The fine compensation can be digitally corrected by a simple digital circuit, which can be built in the timing controller or the column driver. The effective color depth is much larger than that of a fully linear data conversion. The areas for one R-DAC and one C-DAC are 0.438 × 1.063 mm² and 0.207 × 0.11 mm² respectively. The simulated results show that the settling time is within 4 μs. The maximum DNL and INL are 0.28 LSB and 0.35 LSB, respectively. The simulated results show that the proposed column driver is suitable for UXGA LCD-TV application.
Figure 7 The simulated output waveforms of three neighboring channels under dot inversion for the RGB digital inputs of ‘111111111’.

Table 1 Performance Summary.

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.35 μm CMOS 2P4M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit number</td>
<td>10 bits</td>
</tr>
<tr>
<td>Power supplies</td>
<td>3.3 V and 5 V</td>
</tr>
<tr>
<td>DC current of one buffer</td>
<td>6 μA</td>
</tr>
<tr>
<td>Settling time</td>
<td>&lt; 4 μs</td>
</tr>
<tr>
<td>Area of R-DACs (4 channels)</td>
<td>0.438 × 1.063 mm²</td>
</tr>
<tr>
<td>Area of C-DACs (4 channels)</td>
<td>0.207 × 0.11 mm²</td>
</tr>
<tr>
<td>Maximum DNL</td>
<td>0.28 LSB</td>
</tr>
<tr>
<td>Maximum INL</td>
<td>0.35 LSB</td>
</tr>
</tbody>
</table>

6. References


