The evolution of compact, lightweight, low-power, and high-quality displays has caused a large demand for liquid crystal display (LCD) drivers, with features such as low power dissipation, high speed, high resolution, and a large output voltage swing. An LCD driver is generally composed of column drivers, gate drivers, a timing controller, and a reference source. Column drivers are especially important, and generally include registers, data latches, digital-to-analog converters (DACs), and output buffers. Among these components, the DACs and output buffers determine the column driver’s speed, resolution, voltage swing, and power dissipation. Furthermore, DACs occupy the largest silicon area of a column driver chip. Because a single chip includes hundreds of DACs and output buffer amplifiers, the DACs and buffers should occupy a small die area, and their static power consumption should be small.

This chapter deals with recently reported DACs for LCD column drivers, focusing on high-resolution and area-efficient DACs. Beginning with an introduction to the LCD column driver, this chapter first examines the commonly used resistor-string DACs (R-DACs) for LCD column driver applications. The subsequent sections describe capacitive DACs and hybrid DACs, such as resistor–capacitor DACs, embedded DACs, DACs with drain current modulation, and DACs with variable-current control interpolation.

19.1 Introduction

In a typical column driver architecture as shown in Fig. 19.1, the column driver should supply high analog voltages to the LCD panel.\(^1\)\(^5\)
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To reduce the power consumption, the power supply of the digital circuit is low voltage. Digital display data are applied to RGB inputs and sampled into input registers. A wide data latch presents one row of serial input pixel data to the inputs of level shifters. The level shifters then boost the digital signals to higher levels. In the DAC of each channel, a voltage level corresponding to a digital subpixel code appears at its output. The output buffers are used to drive the highly capacitive data lines of the LCD panel.\textsuperscript{6–13}

To improve the lifetime of the liquid crystal material, the liquid crystals of active matrix liquid crystal displays (AMLCDs) should be driven by the so-called inversion method, which alternates positive and negative polarities between the liquid crystal cells with respect to a common backside electrode. Designers use four inversion methods for AMLCD driving: frame, line, column, and dot inversions. High-quality displays prefer the dot inversion method.
Figure 19.2 schematically shows the operation of the dot inversion method. In this method, the backside electrode is at a fixed voltage, and a negative-to-positive or positive-to-negative voltage with respect to the fixed voltage of the backside electrode must be driven from the LCD column drivers with alternating polarities between data lines and line times. Hence, the LCD driver IC should supply both positive and negative polarity voltages for a digital subpixel code. This increases the resolution of the DAC by one bit, and hence increases the die area.

Figure 19.3 (a) shows the characteristic transmittance–voltage curve of the liquid crystal (LC), which exhibits a nonlinear response to the applied voltage. To obtain a linear luminance output with the digital input code for the LCD, the response of the DAC is usually designed to be the inverse of the LC characteristic, as shown in Fig. 19.3 (b). The output of the DAC should cover the positive and negative polarity voltages. R-DACs are usually utilized in LCD driver ICs. Because the transmittance response of the LC to applied voltage is nonlinear, a nonlinear DAC is needed to obtain a linear transmittance with the digital code. To compensate for the nonlinear LC characteristic, gamma correction voltages are applied to the resistor string of the R-DAC and the resistor string is made up of unequal resistors to fit
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![Diagram of Digital circuits, Metal lines and decoders, Buffers](image)

The layout of a typical column driver.

The nonlinear curve. However, the area of the R-DAC and its metal routing will be prohibitively large for a high-resolution data converter. This makes the R-DAC impractical for use in column driver integrated circuits (ICs) for high color depth displays. As an alternative, an LCD column driver using a linear switched capacitor DAC has been proposed. In that case, the nonlinear LC characteristic is compensated for by the timing controller, and the die area is greatly reduced.

The layout of a typical column driver is depicted in Fig. 19.4. The global resistor string, which is inserted in the center of the chip, supplies the reference voltages to all channels. Each channel needs a decoder to route the reference voltage—corresponding to the digital input code—to the corresponding output buffer. Since several hundreds of channels are built into a single chip, the die area of the routing lines, used to connect the resistor string and the decoders, is very large. For example, 2048 metal lines are needed in a 10-bit column driver IC. Hence, the metal lines and decoders will occupy a very large percentage of the column driver IC’s area, especially for high color depth displays.

19.2 Resistive-String DACs

In general, R-DACs are predominantly used for LCD column drivers. The R-DAC consists of a global resistor string in the column driver IC and a decoder in each output channel, as shown in Fig. 19.5. An $n$-bit R-DAC can be realized by using a string of $2^n$ resistors and a $2^n$-to-1 decoder. The global resistor string generates $2^n$ reference voltages and the decoder selects one of the generated reference voltages corresponding to the digital image data to the output through the buffer amplifier. To fit the LCD panel nonlinear characteristic, some gamma voltages are applied to the resistor string and the resistor string is made up of unequal resistors.

The R-DAC has guaranteed monotonicity and can be used for converters up to 10-bit resolution. However, for high-resolution applications, the switch components of the decoder grow exponentially
with the number of bits, causing a larger RC delay at the output and a prohibitively large area of switch components and the metal routing lines. This makes R-DACs impractical for use in the column driver IC for high color depth displays.

Two types of matrix MOS switches are commonly used as the decoder in the conventional R-DAC. Figure 19.6 shows a tree-type decoder DAC. The switch matrix is connected in a treelike manner, eliminating the need for a digital decoder. For an $n$-bit resolution, $2^{n+1} - 2$ switch components are needed. The selected voltage propagates
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**Figure 19.7**

Digital-decoder R-DAC.

From Holding Latches

\[ n \]

\[ n \to 2^n \text{ decoder} \]

Global Resistor String

\[ V_H \]

\[ V_L \]

LCD Panel

through \( n \) levels of switches before arriving at the buffer amplifier. For a high-resolution converter, the switch network may cause a serious delay. For high-speed applications, the tree-type decoder is replaced with a digital decoder shown in Fig. 19.7. In this structure, even though the common node of all the switches is connected to the buffer amplifier, producing a large capacitive load, the selected voltage propagates through a single switch, so that the digital-type converter operates more quickly. However, the area of the digital-type decoder is much larger than that of the tree-type decoder in a high-resolution converter. Therefore, hybrid DAC schemes may be used to restrict the chip area increase.

### 19.3 Resistor–Capacitor DACs

Lu et al.\(^6\) proposed a resistor–capacitor DAC (RC-DAC) that consists of a six-bit R-DAC and a four-bit capacitor DAC (C-DAC) to reduce the driver chip area and to increase the resolution for a higher color depth display. A thin film transistor (TFT)-LCD driver IC should supply both positive and negative polarity voltages for the same digital input. Hence, 124 reference voltages are needed for the six-bit R-DAC. A resistor string is used to generate these 124 reference voltages. The gamma voltages are applied to the resistor string, and the resistor values can be made unequal to compensate for the nonlinear LC characteristic. The coarse gamma correction is made by the external reference voltages, and the fine compensation is adjusted by a simple digital circuit, which can be built into the timing controller or the column.
driver. The characteristic of the C-DAC is linear. Hence, the characteristic of the hybrid DAC is piecewise linear.

Since the column driver IC should drive the LCD with positive and negative polarities, the DACs and output buffers are classified into positive and negative components. Figure 19.8 shows the data conversion scheme. Each channel contains one six-bit R-DAC decoder, one four-bit C-DAC, and one buffer. Two neighboring channels, in which one channel is responsible for driving positive polarity and
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the other for driving negative polarity, are grouped and take turns to drive a pair of adjacent data lines of the LCD panel. The odd DACs and buffers are designed to be used for the negative polarity operation while the positive polarity operation is driven by the even DACs and buffers.

When the odd column lines are under negative polarity and the even column lines are under positive polarity, the input codes and the output buffers are in a normal order. However, when the polarities of the column lines are exchanged, that is, the odd and even column lines are alternated to positive and negative polarities, respectively, the orders of the input codes, DACs, and output buffers are exchanged. The odd DACs still take responsibility for negative polarity operation (and vice versa for the even DACs).

The data conversion is serially implemented by the R-DAC and C-DAC. The decoder for the R-DAC selects two neighboring voltages from the resistor string according to the six most-significant bits (MSBs) and sends them to the C-DAC. Then, the C-DAC uses the two neighboring voltages for the voltage division based on the four least-significant bits (LSBs) and passes the final voltage to the buffer.

The C-DAC, as shown in Fig. 19.9, consists of a parallel-to-serial converter, four switches, and two capacitors. The two capacitors have the same value. The digital data are serially applied to the switches SW1 and SW2. The conversion is performed one bit at a time, resulting in four cycles required for each conversion. For the first cycle, $V_i$ is sampled to $C_2$. The conversion is performed one bit at a time, resulting in four cycles required for each conversion. For the first cycle, $V_i$ is sampled to $C_2$. For each subsequent cycle, a switch is opened and another switch is closed, and the final voltage $V_{out}$ is passed to the buffer.
At the same time, \( V_i \) or \( V_i+1 \), which depends on the input bit, is read to \( C_1 \). Then, the voltages of \( C_1 \) and \( C_2 \) are averaged by turning on SW4. For the other three cycles, a new voltage (\( V_i \) or \( V_i+1 \)) is read to \( C_1 \). Then, SW4 performs the average operation for the voltages of \( C_1 \) and \( C_2 \). The output voltage at the end of the fourth cycle of the conversion can be written as

\[
V_{out} = V_i + \sum_{k=0}^{3} \left( b_k V_{i+1} + b_k V_i \right) - V_i \tag{19.1}
\]

### 19.4 Piecewise Linear DACs

Recently, piecewise linear DACs were utilized in the column driver to reduce the die area and increase the resolution for a higher color depth display. The voltage curve of the piecewise linear DAC is very close to that of the reverse LC response, so these two curves look like identical. As a result, the piecewise gamma correction became possible without losing effective bit resolution.

Lu et al.\(^\text{17}\) presented a 10-bit LCD column driver consisting of piecewise linear DACs. This scheme utilizes a piecewise linear compensation mechanism in the proposed column driver to reduce the die area and increase the resolution for a higher color depth display. This design applies gamma voltages to the resistor string of the R-DAC, and uses unequal resistor values to compensate for the nonlinear LC characteristic.

Figure 19.10 shows the characteristic of the piecewise linear DAC and the reverse response of the LC, where \( V_{G1}, V_{G2}, \ldots, V_{G16} \) are the...
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external gamma reference voltages. The voltage curve of the piecewise linear DAC is very close to that of the reverse LC response, so these two curves look identical. Since the characteristic curve of the piecewise linear DAC is much closer to the inverse response of an LC than a fully linear DAC, fewer additional bits are needed to compensate for the nonlinear LC response. Therefore, the effective color depth is much greater than that of a fully linear data conversion. External reference voltages make coarse gamma correction, and a simple digital circuit makes fine compensation adjustments. This digital circuit can be built in the timing controller or the column driver.

Since the proposed column driver IC drives the LCD with positive and negative polarities, the DACs and output buffers are classified into positive and negative components. Figure 19.11 shows the data conversion scheme. Each channel contains one R-DAC decoder, one C-DAC, and one buffer. Two neighboring channels are grouped together, and take turns driving a pair of adjacent data lines of the LCD panel. One channel is responsible for driving positive polarity and the other for driving negative polarity. The odd DACs and buffers are designed for the negative polarity operation, while the even DACs and buffers drive the positive polarity operation. When the odd channel

Fig. 19.11

Figure 19.11 Data conversion scheme.
lines are under negative polarity and the even column lines are under positive polarity, the input codes and the output buffers are in a normal order. However, when the polarities of the column lines are exchanged—that is, the odd and even column lines are alternated to positive and negative polarities, respectively—the orders of the input codes, DACs, and output buffers are exchanged. The negative buffers and the odd DACs still take responsibility for negative polarity operation, and vice versa for the positive buffers and the even DACs. This arrangement reduces the number of decoder bits by one. In other words, only 10-bit decoders are needed for a 10-bit column driver.

The DAC includes a coarse section and a fine section to reduce both the die area and the data conversion time. The ten-bit DAC in this study contains a seven-bit coarse section and a three-bit fine section implemented by R-DACs and C-DACs, respectively. One resistor string generates the voltage references for all R-DACs in a column driver. Since the DACs cover the positive and negative polarities, the column driver requires an eight-bit resistor string. Each channel contains one seven-bit nonlinear R-DAC and one three-bit linear C-DAC. Reducing the bit number from eleven to seven greatly reduces the area of the R-DACs.

Data conversion is serially implemented by the R-DAC and C-DAC. The R-DAC decoder selects two neighboring voltages according to the seven MSBs and sends them to the C-DAC. The C-DAC then uses the two neighboring voltages to perform voltage division and passes the final voltage to the buffer.

The voltage division in the C-DAC is based on precharging and charge redistribution. Figure 19.12 shows the schematic of the C-DAC.
which consists of three binary weighted capacitors, an additional unit capacitor, and a set of switches that can connect the capacitors to the input voltages. Two phases are needed to accomplish the voltage division in this circuit. In the precharge phase \((f = 0)\), the weighted capacitors are connected to \(v_{i+1}\) or \(v_i\) depending on the three-bit code \((b_2 \sim b_0)\). In the evaluation phase \((f = 1)\), all capacitors are disconnected from the inputs and connected to the output. A charge-redistribution then occurs, and the reconstructed analog value finally appears at the output. The output voltage can be expressed as

\[
v_{\text{out}} = 2^2 \cdot (v_{i+1}b_2 + v_i\bar{b}_2) + 2 \cdot (v_{i+1}b_1 + v_i\bar{b}_1) + (v_{i+1}b_0 + v_i\bar{b}_0) + v_i
\]

\[
= \frac{(4b_2 + 2b_1 + b_0)}{8} (v_{i+1} - v_i) + v_i \tag{19.2}
\]

Equation (19.2) shows that the C-DAC divides the voltage for each segment voltage of the R-string and exhibits a three-bit DAC behavior.

### 19.5 Area-Efficient R-DAC with Polarity Inverter

Lu et al. proposed an area-efficient, fully R-DAC–based thin-film transistor liquid crystal display (TFT-LCD) column driver in which the DACs supply only negative polarity voltages, while polarity inverters generate the positive polarity voltages from the negative polarity voltages. An offset cancellation technique is employed in the negative polarity buffers and polarity inverters.

To compensate for the nonlinear characteristic of LC, DACs should supply the inverse gamma voltages with respect to the LC characteristic. Figure 19.13 shows the inverse gamma curves for demonstrating the proposed driving scheme, where the curves \(P\) and \(N\) represent the positive and negative polarity voltages, respectively. The curve \(P\)

![Image of positive polarity curve](image-url)
can be inverted from its image curve $P$ which is located in the negative polarity region. Many inverse gamma curves of LCD drivers are asymmetric. Hence, the curves $P$ and $N$ do not overlap. Since the inverse gamma curve can be inverted from its image curve, it is possible to eliminate the positive polarity DACs (PPDACs) by generating the positive polarity voltages from the negative polarity voltages.

Figure 19.14 shows the proposed architecture of the $m$-bit fully R-DAC–based column driver, which consists of shift registers, input registers, latches, level shifters, negative polarity DACs (NPDACs), negative polarity buffers, and polarity inverters. The polarity inverters generate the positive polarity voltages, drive the column lines, and replace the PPDACs and positive polarity buffers. This approach groups two driving circuit channels to drive a pair of adjacent column lines. One channel drives negative polarity and the other channel drives positive polarity. Each pair of adjacent channels shares only one level shifter and one $m$-bit NPDAC. Since the proposed driving scheme does not use PPDACs, the rail-to-rail input amplifiers are not essential in the negative polarity buffers and polarity inverters.

A few reference voltages, $V_{refn1}$, $V_{refn2}$, ..., and $V_{refp1}$, $V_{refp2}$, ..., which are generated from a reference IC and transmitted to the resistor
string of DACs through SW2, are used to tune the tap voltages so the
DAC output curve can fit the LCD panel nonlinear characteristic. The
voltages $V_{\text{ref}1}$, $V_{\text{ref}2}$, ..., are negative reference voltages, which fit
the negative inverse gamma curves. The voltages $V_{\text{ref}p1}$, $V_{\text{ref}p2}$, ..., fit the image of the positive inverse gamma curve. If the values of
$V_{\text{ref}p}$ and $V_{\text{ref}n}$ are equal, the DAC characteristic is symmetrical to the
skewed common voltage. To generate an asymmetrical characteristic
curve, the values of $V_{\text{ref}p}$ and $V_{\text{ref}n}$ are set to be unequal. In this case, as
Fig. 19.13 indicates, the voltage, $V_{\text{ref}p}$, applied to the NPDACs should
be $2V_{\text{com}}' - V_{\text{ref}p}$, where $V_{\text{com}}'$ is the skewed common voltage and $V_{\text{ref}p}$
is the reference voltage used to fit the positive inverse gamma curve
for conventional drivers.

Digital display data are applied to the RGB inputs and sampled
into the input registers. The latches output one row of serial input
pixel data to the inputs of level shifters. When the odd column lines
are driven by negative polarity, and the adjacent even column lines
are under positive polarity, the signal, pol, is low. The odd and even
column lines are switched to the outputs of the negative polarity buffers
and the polarity inverters, respectively. When the polarities of the
column lines are exchanged, the negative polarity buffers drive the
even column lines to negative polarity voltages, and the polarity in-
verters drive the odd column lines to positive polarity levels. Each
polarity driving operation is divided into two phases: sample and
hold/driving phases for the negative polarity buffers, and reset and
inversion/driving phases for the polarity inverters.

When the odd column lines are driven by negative polarity and the
adjacent even column lines are under positive polarity, the switches
SW1 and SW2 are set at the “1” position in the first phase, and then
switched to the “0” position in the second phase. In the first phase,
the data from the odd latches are transmitted to the level shifters.
The level shifters then boost the digital signals to higher levels for the
NPDAC inputs.

The negative reference voltages, $V_{\text{ref}n1}$, $V_{\text{ref}n2}$, ..., are applied to
the NPDACs. The voltage levels corresponding to the digital subpixel
codes appear in the NPDAC outputs, and are sampled by the negative
polarity buffers. In this first phase, the polarity inverters are under the
reset phase. In the second phase, the data from the even latches are
transmitted to the NPDACs through the level shifters. The reference
voltages, $V_{\text{ref}p1}$, $V_{\text{ref}p2}$, ..., fitting for the image of positive inverse
gamma curves, are applied to the NPDACs.

The image voltage levels of the positive inverse gamma curve
corresponding to the digital subpixel codes of the even latches then
appear in the inputs of the polarity inverters. In this second phase,
the polarity inverters convert these image voltage levels to positive
inverse gamma voltage levels and drive the even column lines, while
the negative polarity buffers drive the odd column lines.
As the column line polarities are exchanged, the negative polarity buffers sample the voltage levels corresponding to the digital subpixel codes of the even latches in the first phase, and drive the even column lines to the held voltages in the second phase. The polarity inverters invert the voltage from the odd latch data and drive the odd column lines to the inverted voltages in the second phase.

Charge-sharing technology reduces the power consumption of column drivers by reducing the average voltage swing using the switches SW3 and SW3. During each first phase, all column lines are isolated from the negative polarity buffers and the polarity inverters, and are then shorted to an external capacitor. Before the end of this first phase, all column lines are equalized to an average voltage. In the second phase, SW3 is “low” and the column lines are connected to the negative polarity buffers or polarity inverters. The negative polarity buffers and polarity inverters continue to drive the column lines to their final values. Charge sharing, sampling of negative polarity buffers, and resetting polarity inverters all occur during the same time slot, as Fig. 19.14 indicates, so the driving period does not increase.

**19.5.1 Negative Polarity DAC**

Figure 19.15 shows the schematic of an NPDAC, in which the resistor string divides the voltage and generates $2^n$ negative voltage segments. The reference voltages $V_{refn1}$, $V_{refn2}$, ..., and $V_{refp1}$, $V_{refp2}$, ... are applied to the resistor string through the switches, which are controlled by the

---

**Figure 19.15**

Schematic of an NPDAC.
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signal SW2, to fit the negative inverse gamma curve and the image of positive inverse gamma curve, respectively.

NMOS and PMOS transistors typically function as switches in the decoders of conventional negative and positive R-DACs, respectively. The die area of a PMOS switch is greater than that of an NMOS switch. This study uses only one NPDAC in a pair of adjacent channels, thus reducing the total number of DACs. Avoiding the need for PMOS switches in DAC decoders further reduces the required die area.

19.5.2 Negative Buffer

Figure 19.16 shows the negative polarity buffer, which is a sample-and-hold with offset cancellation. Since a pair of adjacent channels shares a single negative polarity DAC, the negative polarity buffer requires a storage capacitor. The terms $C_S$ and $R_Z$ represent the storage capacitor and the compensation resistor, respectively. The same capacitor, $C_S$, is also used for the offset cancellation, and no additional capacitor is required for the offset cancellation. The SW4 and SW5 switches provide unity-gain feedback. To support the offset cancellation, the inverting and noninverting input terminals of the op-amp are exchangeable. As described above, the negative polarity buffer operation can be divided into two phases: sample and hold/driving. Figures 19.17 (a) and (b) show the operations for these two phases.

**Figure 19.16**

Negative polarity buffer.
During the sample phase, SW2 is switched to position “1”, SW4 is turned on, and SW3 and SW5 are turned off. This yields the equivalent circuit shown in Fig. 19.17 (a). The noninverting input terminal is located at the input node, and the inverting input terminal is located at one end of the compensation resistor. The DAC output is connected to the op-amp’s noninverting input terminal. The op-amp is disconnected from the column line and forms a unity-gain buffer. Since the storage capacitor loads the op-amp, the compensation resistor $R_Z$ is inserted between the storage capacitor and the output of the op-amp for stability. Section 19.5.4 explains $R_Z$ in greater detail. The $V_{DAC}$ term represents the input voltage, and $V_{OS}$ is the input-referred offset voltage of the op-amp. For a high-gain op-amp, the voltage at the inverting input terminal, $V_{in-}$, becomes

$$V_{in-} = V_{DAC} - V_{OS}$$  \hspace{1cm} (19.3)$$

The storage capacitor stores the $V_{DAC} - V_{OS}$ voltage.

In the hold/driving phase, the inverting and noninverting input terminals of the op-amp are exchanged. SW2 is switched to the position “0”, SW4 is turned off, and SW3 and SW5 are turned on.
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Figure 19.17 (b) shows that this results in another negative feedback loop. The op-amp is isolated from the DAC and its output is connected to the column line. The stored voltage $V_{DAC} - V_{OS}$ on the storage capacitor $C_S$ becomes the input to the buffer. The output voltage of the buffer, $V_{out}$, becomes

$$V_{out} = V_{DAC} - V_{OS} + V_{OS} = V_{DAC}$$

which demonstrates that the offset voltage is cancelled.

### 19.5.3 Polarity Inverter

Figure 19.18 depicts the polarity inverter and its control signals. The inverter is a switched-capacitor circuit, and the two capacitors $C_1$ and $C_2$ have the same value. The capacitors of $C_1$ and $C_2$ are also used for the offset cancellation. No additional capacitor is required for the offset cancellation. The op-amp is identical to the one used in the negative polarity buffer, and its inverting and noninverting input terminals are also exchangeable. The operation of the polarity inverter is divided into reset and inversion/driving phases, which have the same periods as the sampling and hold/driving phases of the negative polarity buffer, respectively.

Figure 19.19 (a) illustrates the noninverting and inverting input terminals for the reset phase. SW2 is switched to the “1” position. The switches of SW6–SW9 are turned on, and SW3 and SW10–SW12 are turned off. This creates a negative feedback loop and disconnects the

![Diagram of polarity inverter and control signals](image-url)
Digital-to-Analog Converters for LCDs

**Figure 19.19**
Operation of the polarity inverter for the (a) reset and (b) inversion/driving phases.

output of the DAC and the column line. The voltage $V'_{\text{com}}$ is applied to the noninverting input terminal. Due to the negative feedback loop, the voltage at the inverting input terminal is $V'_{\text{com}} - V_{OS}$. The input referred offset voltage of the op amp, $V_{OS}$, is then stored in the two capacitors $C_1$ and $C_2$. The stored charge is

$$Q_1 = Q_2 = V_{OS}C$$  \hspace{1cm} (19.5)$$

where $C$ is the capacitance value of $C_1$ and $C_2$.

In the inversion/driving phase, the inverting and noninverting input terminals of the op-amp are exchanged, as Fig. 19.19 (b) indicates. SW2 is switched to the “0” position. The switches SW3 and SW10–SW12 are turned on, and SW6–SW9 are turned off. This forms another negative feedback loop with the capacitor $C_2$, with its output connected to the column line. The input voltages, $V'_{\text{com}} - V_a$, and $V'_{\text{com}}$ are applied to the bottom plate of $C_1$ and to the noninverting input terminal, respectively, which causes the charge transfer from $C_2$ to $C_1$. The negative feedback through $C_2$ drives the voltage at the top plate of $C_1$ to $V'_{\text{com}} + V'_{OS}$, so that the charge increment on $C_1$ becomes

$$\Delta Q = \left[ (V'_{\text{com}} + V_{OS}) - (V'_{\text{com}} - V_a) \right] C - V_{OS}C = V_aC$$ \hspace{1cm} (19.6)$$

which has been transferred from $C_2$. This reduces the charge across $C_2$ to

$$Q_2 = V_{OS}C - V_aC = (V_{OS} - V_a)C$$ \hspace{1cm} (19.7)$$
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and the output voltage equals

\[ V_{\text{out}} = V'_{\text{com}} + V_{\text{OS}} - (V_{\text{OS}} - V_a) = V'_{\text{com}} + V_a \]  

(19.8)

which is the positive polarity voltage and is symmetric to the input voltage of \( V'_{\text{com}} - V_a \). This approach generates positive inverse gamma voltages based on their image levels.

As for any switched-capacitor circuit, two mechanisms in a MOS transistor operation, such as clock feedthrough and channel charge injection, introduce error in the polarity inverter at the instant the switch turns off. Since a constant skewed common voltage is applied to the polarity inverter in the first phase, the channel charges of SW6–SW9 result in a constant offset voltage. This offset voltage, which is independent of the input voltage, can be compensated for by adjusting the value of the skewed common voltage, \( V'_{\text{com}} \).

Two techniques can reduce the effect of clock feedthrough and charge injection. A dummy switch can remove the charge injected by the main switch transistor. Another approach to lowering the effect of charge injection incorporates both PMOS and NMOS devices so the opposite charge packets injected by the two devices cancel each other. In this work, the complementary switches are used to reduce the charge injection.

19.5.4 Operational Amplifier

A high color depth LCD driver requires a high-gain and large-driving op-amp to drive the large capacitive load of the column line. Since the proposed driving scheme does not use PPDACs, the rail-to-rail input amplifiers are not essential in the negative polarity buffers and polarity inverters. Figure 19.20 shows a schematic of a three-stage op-amp. The transistors M1–M5, M6–M10, and M11–M12 compose the first, second, and third stage, respectively. The first two stages are differential amplifiers, and the last stage is a complementary common-source amplifier. Since the first and second differential amplifiers bias the output transistors M12 and M11, respectively, the output stage has a large push–pull driving capability. The switches reverse the input polarities of the op-amp. The capacitor \( C_{\text{cs}} \) is used for Miller compensation.

In the stable state, the inverting input voltage is equal to the noninverting input voltage. The currents flowing in M9 and M10 are equal to \( I_{b2}/2 \), where \( I_{b2} \) is the bias current of the second differential amplifier. The gate voltage of M11 is equal to that of M9. The quiescent current of M11 is then the current \( I_{b2}/2 \) times their corresponding transistor size ratio. That is,

\[ I_{11} = \left( \frac{W}{L} \right)_{11} \cdot \frac{I_{b2}}{2} \]  

(19.9)
The total quiescent current $I_{\text{tot}}$ of the amplifier is:

$$I_{\text{tot}} = I_{b1} + \left(1 + \frac{(W/L)_1}{2(W/L)_2}\right)I_{b2} \tag{19.10}$$

where $I_{b1}$ is the bias current of the first differential amplifier.

Swapping the output terminals from the first-stage differential amplifier reverses the input polarity of the op-amp. When the signal $S$ is high, the drain ends at M4 and M5 connect to the gates at M8 and M7, respectively. The input terminals $\text{in1}$ and $\text{in2}$ are noninverting and inverting, respectively. The signal $S$ is low when the connections between the first-stage amplifier outputs and the second-stage amplifier inputs are swapped. This reverses the input polarity. However, the input referred offset voltage maintains the same polarity, as Figs. 19.17 and 19.19 indicate.

19.6 Conclusions
DACs for LCD systems play the key role of data voltage generation. The stringent requirements of DACs for LCD-driver ICs are as follows: a uniform characteristic in output channels, compactness in silicon die area, and low power consumption. Recent improvements in LCD panels for multimedia and medical products allow higher definition
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and greater color depth. Achieving the higher color depths that LCD drivers can produce requires a higher resolution in DACs.

In general, nonlinear R-DACs are predominantly used for LCD column drivers. Their prevalence is partly because of their uniform characteristics, because each output channel of the column driver IC shares a global resistor string for reference voltage generation. However, for high-resolution applications, the switch components of the decoder grow exponentially with the number of bits, causing a prohibitively large area of switch components and metal routing lines. This makes R-DACs impractical for use in the column driver IC for high color depth displays.

Another alternative for nonlinear DACs is linear DACs. The linear DAC topology allows independent gamma control for red, green, and blue colors, which provides more vivid colors over all gray levels without the tremendous increase in chip area that is expected in R-DAC architecture. However, the data driver with linear DACs will lose at least two bits from its effective bit resolution since additional bits are necessary to compensate for the nonlinear LC characteristic.

Piecewise linear DAC architectures with nonlinear R-DACs have been introduced to make the most of the nonlinear R-DAC for its nonlinear gamma correction, which is made possible without loss of effective bit resolution.

References

Digital-to-Analog Converters for LCDs
